

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Luz Alejandro Examiner #: 71110 Date: 10/02/02
 Art Unit: 1763 Phone Number 303-4545 Serial Number: 091519719
 Mail Box and Bldg/Room Location: 10 834 Results Format Preferred (circle) PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Temperature controlled semiconductor processing chamber

Inventors (please provide full names): ① Hamid Nourbakhsh, ② Siamak Salimian, ③ Paul Lusch
④ James D. Carducci, ⑤ Evans Lee, ⑥ Kaushik Vaidya, ⑦ Hongging Shan, ⑧ Michael D. L

Earliest Priority Filing Date: 03/07/2000

For Sequence Searches Only Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

Please refer to claims 11-15, 21-28 and 37-52* for specific limitations to be searched.

*claims are in the attached copy

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	Type of Search	Vendors and cost where applicable
Searcher: <u>ST</u>	NA Sequence (#) _____	STN <u>P 142.64</u>
Searcher Phone #: _____	AA Sequence (#) _____	Dialog _____
Searcher Location: _____	Structure (#) _____	Questel/Orbit _____
Date Searcher Picked Up: _____		

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S/N 09/519,719
4150/ETCH/DRIE/JB1

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant: Noorbakhsh, et al.

Case: 4150

Serial No.: 09/519,719

Filed: March 7, 2000

Examiner: Alejandro Mulero

Group Art Unit: 1763

Title: **TEMPERATURE CONTROLLED SEMICONDUCTOR PROCESSING
CHAMBER LINER**

ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

SIR:

AMENDMENT

In response to the Office Action dated October 11, 2001, 2001 (Paper No. 4), please amend the above-identified patent application as follows:

IN THE CLAIMS

Please replace the indicated claims as follows:

11. (AMENDED) A semiconductor processing chamber comprising:
- a wall, a bottom and a lid assembly defining a chamber volume;
 - a substrate support disposed within the chamber volume; and
 - ^{Al₂O₃ ceramic stainless} a chamber liner disposed in the chamber volume and circumscribing the substrate support, the chamber liner having a passage at least partially disposed in the chamber line, the passage fluidly isolated from the chamber volume and having an inlet and outlet adapted to flow a fluid through the passage.

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26. (AMENDED) Apparatus for lining a semiconductor processing chamber comprising:

A2 a liner having a plurality of ^{perforated} apertures formed at least partially therein;

a lid having an inlet, the lid disposed proximate the liner and defining a plenum at least partially therebetween; and

a nozzle disposed in at least one of apertures.

Please added the following claims:

--37. (NEW) The apparatus of claim 25, wherein the second side of the liner is textured.

A3 38. (NEW) Apparatus for lining a process volume defined by sidewalls of a semiconductor processing chamber comprising:

a liner adapted to be removably disposed in the process volume; and

a passage at least partially formed in the liner isolated from the process volume and adapted to flow a heat transfer medium therethrough.

39. (NEW) The apparatus of claim 38, wherein the liner further comprises:
a cylindrical wall.

40. (NEW) The apparatus of claim 39, wherein the passage is formed at least partially in the cylindrical wall.

41. (NEW) The apparatus of claim 39, wherein the liner further comprises:
a bottom coupled to the cylindrical wall.

42. (NEW) The apparatus of claim 41, wherein the passage is formed at least partially in the bottom.

43. (NEW) The apparatus of claim 39, wherein the cylindrical wall is configured to line the sidewalls to the chamber.

44. (NEW) The apparatus of claim 39, wherein the cylindrical wall is configured to line a substrate support disposed in the process volume of the chamber.

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45. (NEW) The apparatus of claim 38, wherein the liner further comprises:
an outer cylindrical wall;
an inner cylindrical wall; and
a bottom coupled between the outer cylindrical wall and the inner cylindrical wall.

46. (NEW) The apparatus of claim 45, wherein the passage is formed in at least partially in at least one of the inner cylindrical wall, outer cylindrical wall and the bottom.

47. (NEW) A semiconductor processing chamber comprising:
a wall, a bottom and a lid assembly defining a chamber volume;
a substrate support disposed within the chamber volume; and,
a chamber liner having at least a first portion disposed proximate the wall, the chamber liner having a passage fluidly isolated from the chamber volume at least partially formed in the chamber liner.

48. (NEW) The chamber of claim 47, wherein the chamber liner further comprises:

a second portion disposed proximate the lid assembly.

49. (NEW) The chamber of claim 48, wherein the second portion of the chamber liner further comprises:

a plurality of apertures formed therethrough.

50. (NEW) The chamber of claim 49 further comprising a plate disposed on the chamber liner and forming a plenum therewith, the plenum in fluid communication with the chamber volume through the apertures.

51. (NEW) A semiconductor processing chamber comprising:

a wall, a bottom and a lid assembly defining a chamber volume;

a substrate support disposed within the chamber volume; and,

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a chamber liner circumscribing the substrate support, the chamber liner having a passage fluidly isolated from the chamber volume at least partially formed in the chamber liner.

52. (AMENDED) Apparatus for lining a chamber volume of a semiconductor processing chamber, comprising:

a liner having a plurality of apertures formed at least partially therein;

a passage at least partially formed in the liner and fluidly isolated from the chamber volume; and

a nozzle disposed in at least one of apertures.--.

REMARKS

This reply is intended as a full and complete response to the Office Action mailed on October 11, 2001. In view of both the amendments presented above and the following discussion, the Applicants believe that all claims are now in allowable form.

RESTRICTION

The Applicants confirm the election made by Todd Patterson on October 3, 2001, to prosecute the invention of Group II, claims 11-28. Claims 1-10 and 29-36 are cancelled without prejudice. The Applicants reserve the right to subsequently file divisional applications in order to prosecute the non-elected group.

Additionally, the Examiner has identified species and generic claims from the elected group. The Applicants confirm the election made by Todd Patterson on October 5, 2001, to prosecute generic claims 11-15 and Specie A, Claims 21-28.

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16. The apparatus of claim 12 wherein the second liner further comprises:
a base having the passage disposed within; and
5 an inner wall connected to the base.
17. The apparatus of claim 16 wherein the second liner further comprises:
an outer wall connected to the base.
- 10 18. The apparatus of claim 16 wherein the second liner further comprises:
a first and second boss projecting from the base, the first boss comprising a hole in fluid communication with the
15 passage at the inlet, and the second boss comprising a hole in fluid communication with the passage at the outlet.
19. The apparatus of claim 16 wherein inner wall further comprises a magnet disposed in the inner wall.
- 20 20. The apparatus of claim 17 wherein the outer wall further comprises a pumping port.
21. The apparatus of claim 12 wherein the first liner further comprises:
25 a center member having the passage disposed within;
a flange circumscribing the center member; and,
a cylindrical wall projecting from the center member inside of the flange.
- 30 22. The apparatus of claim 21 further comprising:
a lid disposed opposite the cylindrical wall, the lid and the wall defining a plenum at least partially therebetween.
- 35 23. The apparatus of claim 22 wherein the center member further comprises:

What is claimed is:

1. A thermally controlled apparatus for lining a semiconductor processing chamber comprising:
5 a base;
an inner wall connected to the base; and,
a passage disposed in the base, the inner wall or the base and the inner wall, the passage having an inlet and outlet.
- 10 2. The apparatus of claim 1 further comprising an outer wall connected to the base.
3. The apparatus of claim 2 wherein the outer wall further
15 comprises a pumping port.
4. The apparatus of claim 1 wherein the inner wall further comprises a magnet disposed in the inner wall.
- 20 5. The apparatus of claim 1 wherein the base is comprised of a material selected from the group of aluminum, ceramic and stainless steel.
6. The apparatus of claim 1 further comprising:
25 a first and second boss projecting from the base, the first boss comprising a hole in fluid communication with the passage at the inlet, and the second boss comprising a hole in fluid communication with the passage at the outlet.
- 30 7. A thermally controlled apparatus for lining a semiconductor processing chamber comprising:
a center member;
a flange circumscribing the center member;
a cylindrical wall projecting from the center member
35 inside of the flange; and
a passage disposed in the center member having an inlet and an outlet.

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a plurality of nozzles disposed in the center member providing fluid access to the plenum.

24. The apparatus of claim 22 further comprising:

- 5 a gas feedthrough fluidly coupled to the plenum through a hole disposed in the lid.

25. Apparatus for lining a semiconductor processing chamber comprising:

- 10 a liner having a plurality of apertures formed at least partially therein; and

a lid having an inlet, the lid disposed proximate the liner and defining a plenum at least partially therebetween.

- 50 15 26. The apparatus of claim 25 further comprising:
a nozzle disposed in each of the plurality of apertures.

27. The apparatus of claim 26, wherein the nozzle is
20 comprised of quartz, silicon carbide, silicon, aluminum nitride, aluminum oxide or combinations thereof.

28. The apparatus of claim 26, wherein the liner further comprises:

- 25 a channel having an inlet and an outlet disposed in the liner.

- 275 29. A nozzle for providing fluid entry to a processing chamber comprising:

- 30 a mounting portion adapted to be couple to the processing chamber; and

a gas delivery portion, the mounting portion and the gas delivery having one or more passages extending through.

- 35 30. The nozzle of claim 29, wherein one of the one or more passages comprises:

a central passage extending at least partially through the mounting portion; and

a lid disposed opposite the cylindrical wall, the lid and the wall defining a plenum at least partially therebetween.

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a plurality of nozzles disposed in the center member providing fluid access to the plenum.

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a gas feedthrough fluidly coupled to the plenum through a hole disposed in the lid.

11. a wall, a bottom and a lid assembly defining a chamber volume,

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and a chamber liner disposed in the chamber volume, the chamber liner having a passage at least partially disposed therein, the passage having an inlet and outlet adapted to flow a fluid through the passage.

a first liner disposed proximate the lid assembly; or
a second liner disposed about the substrate support.

30 13. The chamber of claim 11 wherein the chamber liner is
retained in the chamber by a clamp affixed to the chamber.

14. The chamber of claim 11 wherein the chamber liner is comprised of a thermally conductive material.

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15. The chamber of claim 11 wherein the chamber liner is comprised of a material selected from the group of aluminum, ceramic and stainless steel.

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FILE 'HCA, WPIX, JAPIO' ENTERED AT 15:28:22 ON 04 OCT 2002

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L6 27631 SEA (CVD OR (CHEMICAL? OR CHEM) (2A) (VAPOR? OR VAPOUR?) (2A))DEPOSIT? OR OMCVD OR MOCVD OR LPCVD OR PECVD OR HFCVD OR ULPCVD OR PACVD OR PCVD) /BI,AB

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TOTAL FOR ALL FILES

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L9 874094 SEA CHAMBER? OR VESSEL? OR REACTOR? OR CONTAINER? OR FLASK?

L10 1043215 SEA CHAMBER? OR VESSEL? OR REACTOR? OR CONTAINER? OR FLASK?

L11 448646 SEA CHAMBER? OR VESSEL? OR REACTOR? OR CONTAINER? OR FLASK?

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L12 2365955 SEA CHAMBER? OR VESSEL? OR REACTOR? OR CONTAINER? OR FLASK?

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L58 52 SEA L54 AND L42
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L62 28 SEA L58 AND (L14 OR L18 OR L22 OR L26 OR L30 OR L34 OR
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L82 655 SEA L78 AND L74
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L127 24 SEA L55 AND L123
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L130 22 SEA L126 AND (L14 OR L18 OR L22 OR L26)
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L153 11 SEA L125 AND L45

L154 12 SEA L126 AND L46
L155 1 SEA L127 AND L47

TOTAL FOR ALL FILES

L156 24 SEA L128 AND L48
L157 2 SEA L125 AND L49
L158 9 SEA L126 AND L50
L159 0 SEA L127 AND L51

TOTAL FOR ALL FILES

L160 11 SEA L128 AND L52

FILE 'HCA' ENTERED AT 16:28:38 ON 04 OCT 2002

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L131 OR L139 OR L143 OR L147 OR L155
L168 7 SEA L167 AND L123
L169 6 SEA L167 NOT L168

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FILE 'JAPIO' ENTERED AT 17:25:33 ON 04 OCT 2002

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FILE LAST UPDATED: 11 SEP 2002 <20020911/UP>

FILE COVERS APR 1973 TO MAY 31, 2002

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L168 ANSWER 1 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 2001-104825 JAPIO

TITLE: HEATED ELECTROSTATIC PARTICLE TRAP FOR CLEANING
IN-SITU VACUUM LINE OF SUBSTRATE TREATING
CHAMBERINVENTOR: TANAKA TSUTOMU; CHOO T NGUYEN; PONNEKANTI HARI;
FAIRBAIRN KEVIN; SEBASTIEN RAOKKUSU; MARK
ANTHONY FODOORU

PATENT ASSIGNEE(S): APPLIED MATERIALS INC

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2001104825	A	20010417	Heisei	B03C003-40

APPLICATION INFORMATION

STN FORMAT: JP 2000-216215 20000717

ORIGINAL: JP2000216215 Heisei

PRIORITY APPLN. INFO.: US 1999-354925 19990715

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 2001

AN 2001-104825 JAPIO

AB PROBLEM TO BE SOLVED: To provide a device and method for preventing
the accumulation of a granular material and residue in a vacuum
discharge line of a **semiconductor treating**
device.SOLUTION: A **vessel chamber** having an
inlet, an **outlet** and a fluid conduit interposed
between them is provided, and the conduit is provided with the first
and the second collecting sections. The first collecting section is
provided with the first plural electrodes lined up in parallel to
the first surface, and the second collecting section is provided
with the **second** plural electrodes lined up in
parallel to the second surface. The electrodes are connected in a
voltage differential mode and electrostatic particle collector is
formed for capturing the granular material and charged particles
flowing through the fluid conduit. The particles are collected on
the electrode in the fluid conduit during the substrate treating
operation such as in **CVD** depositing step.

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IC ICM B03C003-40

ICS B01J003-02; B03C003-08; B03C003-09; B03C003-14; B03C003-66;
C23C016-44; H01L021-205

L168 ANSWER 2 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1999-067746 JAPIO

TITLE: CONTROL OF OXYGEN/SILANE RATIO IN SEASONING
PROCESS FOR IMPROVING PARTICLE CHARACTERISTIC IN
HOP-**CVD** DEVICEINVENTOR: QIAO JIANMIN; CHAN CHIU; CHAN DIANA; LEUNG CISSY
S; TURGUT SAHIN

PATENT ASSIGNEE(S): APPLIED MATERIALS INC
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 11067746	A	19990309	Heisei	H01L021-31

APPLICATION INFORMATION

STN FORMAT: JP 1998-180770 19980626
 ORIGINAL: JP10180770 Heisei
 PRIORITY APPLN. INFO.: US 1997-887239 19970702
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
 Applications, Vol. 1999

AN 1999-067746 JAPIO

AB PROBLEM TO BE SOLVED: To decrease the level of contaminant such as particles generated in a seasoning layer deposited on a part of the inner surface of a **chamber** by forming plasma from the gas flow of oxygen (O<SB>2</SB>) and silane (SiH<SB>4</SB>) introduced into the **chamber** so that the specified flow-rate ratio is obtained, and performing the control carefully.
 SOLUTION: In order to assure the excellent deposition of a deposited film on the inner surface of a **chamber**, many deposition parameters including temperature, pressure, RF electric-power levels, the ratio of argon and O<SB>2</SB> and the ratio of O<SB>2</SB> and SiH<SB>4</SB> are controlled. When the flow-rate ratio of O<SB>2</SB> when the SiH<SB>4</SB> of seasoning gas is made to be 1 is 1.4-2.4, the seasoning film generated as a result indicates the improved deposition property for the surface of ceramic or the like, where deposition is difficult. More suitably, the flow-rate ratio of O<SB>2</SB> when SiO<SB>4</SB> is 1 should be 1.6-2.2. The number of particles and the contamination level in a substrate processing device including the inner surface, which is at least partially **lined** with the **ceramic**, can be decreased.

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IC ICM H01L021-31
 ICS H01L021-3065

L168 ANSWER 3 OF 7 JAPIO COPYRIGHT 2002 JPO
 ACCESSION NUMBER: 1998-223619 JAPIO
 TITLE: METHOD OF TREATING
 SEMICONDUCTOR WAFER
 INVENTOR: KARL EMERSON MOTZ
 PATENT ASSIGNEE(S): MOTOROLA INC
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 10223619	A	19980821	Heisei	H01L021-3065

APPLICATION INFORMATION

STN FORMAT: JP 1998-33772 19980130

ORIGINAL: JP10033772 Heisei
PRIORITY APPLN. INFO.: US 1997-794698 19970203
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 1998

AN 1998-223619 JAPIO

AB PROBLEM TO BE SOLVED: To provide a method of **treating semiconductor wafer** which reliably removes particles from a treating **chamber** and substrate surface in a treating cycle, without adding a long time.
SOLUTION: A treating **chamber** 210 has an isolation region 252. An electrically controlled grid 250 is inserted between the region 252 and **liner** 220 and has independently voltage-controllable segments 250a, 250b, 250c, 250d. Power is fed between treating steps of a semiconductor substrate 230 to attract particles 235 floating in the **chamber** 210 toward the grid 250 away from the substrate. While a gas flow or pressure lowering is made in the treating **chamber** the voltage on the grid is changed to move the particles 235 to a pumping **port** 239 owing an electric force and remove the particles through this **port** from the **chamber**.
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IC ICM H01L021-3065
ICS H01L021-68

L168 ANSWER 4 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1998-070112 JAPIO

TITLE: APPARATUS AND METHOD FOR CLEANING
SEMICONDUCTOR TREATING CHAMBER SURFACE

INVENTOR: ROBERT J SUTEGAA; FRED C REDEKAA

PATENT ASSIGNEE(S): APPLIED MATERIALS INC

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 10070112	A	19980310	Heisei	H01L021-31

APPLICATION INFORMATION

STN FORMAT: JP 1997-153946 19970611
ORIGINAL: JP09153946 Heisei
PRIORITY APPLN. INFO.: US 1996-661842 19960611
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 1998

AN 1998-070112 JAPIO

AB PROBLEM TO BE SOLVED: To prevent a semiconductor from contamination with deposits remaining in a **chamber**.
SOLUTION: The temp. of a **temp.-controlled ceramic liner** 102 near the surface of a **chamber** 100 is set to reduce the deposit forming on the **liner** surface or accelerate the deposit removing from the **liner** surface during **treating** a **semiconductor** substrate. Some deposit may early grow on the

chamber surface. Forming and removing rates of the deposit depend on the temp. and the **liner** 102 can be made so as to independently set the temp. at different places. In case of a plurality of **temp.-controllable liners** 102, they set to different temps. according to the requirements for reducing the forming of the deposit on regions of the **chamber** 100 protected with the **liners** and for removing the deposit. A plasma generated outside the **chamber** 100 is pref. fed into the **chamber** through a conduit at treating or cleaning of the substrate. At least the inner surface of the conduit to contact with the plasma is made of a halogen-containing material; the halogen is selectable according to the active species passing through the conduit.

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IC ICM H01L021-31

ICS H01L021-02; H01L021-203; H01L021-205; H01L021-3065

L168 ANSWER 5 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1997-251992 JAPIO

TITLE: METHOD FOR REDUCING RESIDUE DEPOSITION IN
CVD CHAMBER USING
CERAMIC LINING AND ITS DEVICE

INVENTOR: SHIYAO JIYUN; TOMU CHIYOO; SHIN SHIEN GUO;
TABATA ATSUSHI; JIYANMIN CHIYAO; ARETSUKUSU
SHIYUREIBAA

PATENT ASSIGNEE(S): APPLIED MATERIALS INC

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 09251992	A	19970922	Heisei	H01L021-31

APPLICATION INFORMATION

STN FORMAT: JP 1996-335940 19961216

ORIGINAL: JP08335940 Heisei

PRIORITY APPLN. INFO.: US 1995-577862 19951222

SOURCE: INPADOC

AN 1997-251992 JAPIO

IC ICM H01L021-31

ICS C23C016-44; C23C016-50; H01L021-205

L168 ANSWER 6 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1990-251136 JAPIO

TITLE: SEMICONDUCTOR WAFER HEAT
TREATMENT DEVICE

INVENTOR: NATORI HIROYUKI

PATENT ASSIGNEE(S): NEC CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 02251136	A	19901008	Heisei	H01L021-22

APPLICATION INFORMATION

STN FORMAT: JP 1989-72532 19890324
ORIGINAL: JP01072532 Heisei
PRIORITY APPLN. INFO.: JP 1989-72532 19890324
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 1990

AN 1990-251136 JAPIO

AB PURPOSE: To facilitate control of impurity diffusion on the surface of each semiconductor wafer as well as the uniform progress of an oxidation film thickness and the like by controlling the flow rate of a gas which is supplied to respective zones in a reactor tube.

CONSTITUTION: A plurality of semiconductor wafers 8 are lined up and loaded in a boat 9 that is inserted in a reactor tube 2 and a gas from a gas feeder 4a is supplied through gas supply ports 5 of three pieces of gas feeding tubes 3 which supply the gas independently to respective front, center, and rear zones of the semiconductor wafers 8. On the basis of electric signals with respect to the gas concentration of each zone which is detected by a gas concentration detector 11, the flow rate of the gas that is supplied to respective zones is controlled by the gas feeder 4a. Impurity diffusion on the surface of each semiconductor wafer as well as the uniform progress of an oxidation film thickness and the like are thus controlled easily.

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IC ICM H01L021-22

L168 ANSWER 7 OF 7 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1989-304613 JAPIO

TITLE: MANUFACTURE OF OXIDE SUPERCONDUCTIVE WIRE ROD

INVENTOR: AOKI SHINYA; KONO TSUKASA; OSANAI YUTAKA;
SHINADA TOMOAKI; SUGIMOTO OSAMU; WATANABE
KIICHIROPATENT ASSIGNEE(S): FUJIKURA LTD
CHUBU ELECTRIC POWER CO INC
CHUGOKU ELECTRIC POWER CO INC:THE
KYUSHU ELECTRIC POWER CO INC

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 01304613	A	19891208	Heisei	H01B013-00

APPLICATION INFORMATION

STN FORMAT: JP 1988-133224 19880531
ORIGINAL: JP63133224 Showa
PRIORITY APPLN. INFO.: JP 1988-133224 19880531
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 1989

AN 1989-304613 JAPIO

AB PURPOSE: To form an oxide superconductor of a homogeneous crystal

structure by forming a mixed material layer including each element that compose a superconductor of oxide on the surface of the base material by means of the chemical evaporation method and providing a heat treatment simultaneously with or after the formation of this material layer.

CONSTITUTION: A superconductive wire rod of oxide provided with oxide superconductor of A-B-Cu-O is formed. This A indicates more than one kind of elements of periodic table group IIIa such as Y, Sc, La, Yb, Er, Eu, Ho, Dy, etc., and B indicates more than one kind of elements of periodic table group IIa such as Be, Mg, Ca, Sr, Ba, etc. A long sized base material 10 of a round **liner** rod is bound to a rolled roll in a vacuum **container** 21 of a plasma **CVD** device, shifted to a roll 26 on the other side and the base material shifted in the evacuated **container** 21 is heated by means of a heater 27. Powder 29 of $\text{BaCo}_{<\text{SB}>3</SB>}$ is transferred from a supply **port** 28 of a plasma generating tube 22 by means of carrier gas at the time of shifting the base material 10, and at the same time, plasma flange 30 is generated toward the base material 10 of the **container** 21 by activating an induction heater 23.

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IC ICM H01B013-00
ICS B21F019-00; B21F019-00; C01B003-00; C04B041-87; C23C016-40;
C23C016-50
ICA H01B012-04

=> d l169 1-6 ibib abs ind

L169 ANSWER 1 OF 6 JAPIO COPYRIGHT 2002 JPO
ACCESSION NUMBER: 2002-141332 JAPIO
TITLE: SEMICONDUCTOR MANUFACTURING EQUIPMENT
INVENTOR: SUGANO SEIICHIRO; NISHIO RYOJI; YOSHIOKA
TAKESHI; KANAI SABURO
PATENT ASSIGNEE(S): HITACHI LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2002141332	A	20020517	Heisei	H01L021-3065

APPLICATION INFORMATION

STN FORMAT: JP 2000-331075 20001030
ORIGINAL: JP2000331075 Heisei
PRIORITY APPLN. INFO.: JP 2000-331075 20001030
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 2002

AN 2002-141332 JAPIO
AB PROBLEM TO BE SOLVED: To provide a process equipment which exhibits a high controllability of the wafer temperature by arbitrarily setting the pressure distribution of thermally conductive gas introduced between a semiconductor wafer and a wafer stage.

SOLUTION: The semiconductor manufacturing equipment is provided with a plasma generating means for generating plasma in a vacuum **processing chamber**, a **wafer stage 6** for holding the semiconductor wafer 5 on its surface, and a **temperature controlling** means 26 for controlling the semiconductor wafer 5. The wafer stage 6 is provided with a first gas **inlet 19** which is placed near the center of the wafer stage 6, a second gas **inlet 27** which is placed near the periphery of the wafer stage 6, and a gas **outlet 31** which is placed on the inner side of the second gas **inlet** of the wafer stage 6. The **temperature controlling** means 26 arbitrarily sets the pressure distribution of the thermally conductive gas by controlling the flow of the gas from the gas **outlet 31**.

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IC ICM H01L021-3065
ICS H01L021-68

L169 ANSWER 2 OF 6 JAPIO COPYRIGHT 2002 JPO
ACCESSION NUMBER: 2002-100624 JAPIO
TITLE: DILUTE REMOTE PLASMA CLEAN
INVENTOR: BALISH KENNETH E; NOWAK THOMAS; TANAKA TSUTOMU;
BEALS MARK
PATENT ASSIGNEE(S): APPLIED MATERIALS INC
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2002100624	A	20020405	Heisei	H01L021-31

APPLICATION INFORMATION

STN FORMAT: JP 2001-124692 20010423
ORIGINAL: JP2001124692 Heisei
PRIORITY APPLN. INFO.: US 2000-553694 20000421
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002

AN 2002-100624 JAPIO

AB PROBLEM TO BE SOLVED: To provide a method and an apparatus for enhancing the etch characteristics of a plasma formed in a remote plasma generator.

SOLUTION: A plasma formed in a remote plasma generator (27) flows through a tube (62) to a **plenum** (60) where it is diluted to form a plasma mixture before the plasma mixture flows into a **processing chamber** (15). The plasma mixture is used to clean deposits from the interior surfaces of the **processing chamber**, or can be used to perform an etch step on a **processed wafer** within the **processing chamber**. In one embodiment, a plasma formed from NF₃ is diluted with N₂ to etch residue from the surfaces of the **processing chamber** used to deposit silicon oxide glass. Diluting the plasma increases the etching rate and makes the etching rate more uniform across the diameter of the **processing chamber**.

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IC ICM H01L021-31
ICS C23C016-44; H01L021-3065

L169 ANSWER 3 OF 6 JAPIO COPYRIGHT 2002 JPO
ACCESSION NUMBER: 2002-057146 JAPIO
TITLE: PLASMA PROCESSING **CHAMBER** AND BAFFLE
PLATE ASSEMBLY
INVENTOR: KINNARD DAVID W
PATENT ASSIGNEE(S): AXCELIS TECHNOLOGIES INC
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2002057146	A	20020222	Heisei	H01L021-3065

APPLICATION INFORMATION

STN FORMAT: JP 2001-128061 20010425
ORIGINAL: JP2001128061 Heisei
PRIORITY APPLN. INFO.: US 2000-558606 20000426
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 2002

AN 2002-057146 JAPIO

AB PROBLEM TO BE SOLVED: To provide a plasma processing **chamber** and a baffle plate assembly for forming a laminar flow of activated gas which crosses a surface of a processing substrate in a plasma processing device.
SOLUTION: A plasma processing **chamber** 10 comprises an inner **chamber** 20 for **wafer processing** formed of a pall 38 with a top wall 17, a lower baffle plate 16 which is disposed adjacent to the inner **chamber** 20 for dispersing activated gas and is almost flat and a baffle plate assembly 12 including an upper baffle plate 14 which is fixed and disposed above the plate 16 and is almost flat. A **plenum** is formed between the top wall 17 and the lower baffle plate 16. The **plenum** works under a higher pressure than the inner **chamber** 20 during operation of the plasma processing **chamber** 10 and the lower baffle plate 16 has a pattern of an opening 30 formed to enable gas to be supplied into an inner **chamber** through a **plenum**.

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IC ICM H01L021-3065
ICS B01J019-08; C25D011-04; G03F007-42; H01L021-027; H05H001-46

L169 ANSWER 4 OF 6 JAPIO COPYRIGHT 2002 JPO
ACCESSION NUMBER: 2001-313264 JAPIO
TITLE: TREATING GAS FILLING **PORT** AND
EXHAUSTING **PORT** STRUCTURE
INVENTOR: ISHII KAORU; WILKINSON THOMAS F; MOROI MASAYUKI
PATENT ASSIGNEE(S): TEXAS INSTR INC <TI>
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2001313264	A	20011109	Heisei	H01L021-205

APPLICATION INFORMATION

STN FORMAT: JP 1989-112664 19891220
ORIGINAL: JP2001112664 Heisei
PRIORITY APPLN. INFO.: US 1988-287106 19881220
PRIORITY APPLN. INFO.: US 1988-287171 19881220
PRIORITY APPLN. INFO.: US 1988-287174 19881220
PRIORITY APPLN. INFO.: US 1988-287418 19881220
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined
Applications, Vol. 2001

AN 2001-313264 JAPIO

AB PROBLEM TO BE SOLVED: To provide a treating gas filling port
and exhausting port structure used together with a
continuously chemical vapor deposition
reactor having a connecting part between reaction
chambers.

SOLUTION: The treating gas filling port and exhausting
port structure is used together with the continuously
chemical vapor deposition
reactor having the connecting part between reaction
chambers. In this case, the connecting part on one end of
the reaction chamber is a gas input connector, and the
connecting part on the other end of the reaction chamber
is a gas exhaust connector. The treating gas filling port
and exhausting port structure comprises a gas
plenum in the gas input connector having a single input gas
filling port, a plurality of gas filling ports
positioned at a side of the plenum opposed to the signal
input gas filling port and disposed to receive a gas of an
equal amount from the input gas filling port to distribute
the gas to the reaction chambers, an exhaust port
of the exhaust connector positioned at the end of the reaction
chamber opposed to the input connector and positioned at a
center with respect to the end of the reaction chamber
adjacent to the exhaust connector, and a shutter for partly closing
the plurality of the gas filling ports to distribute the
gas to the reaction chambers.

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IC ICM H01L021-205

ICS C23C016-455

L169 ANSWER 5 OF 6 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1999-044443 JAPIO

TITLE: CLEAN ROOM, MANUFACTURE OF SEMICONDUCTOR
ELEMENT, TREATING CHAMBER
FOR MANUFACTURING SEMICONDUCTOR ELEMENT,
MANUFACTURING DEVICE FOR SEMICONDUCTOR ELEMENT
AND CLEANING METHOD OF MEMBER FOR SEMICONDUCTOR
ELEMENT

INVENTOR: TAKAHASHI MASAHIRO
 PATENT ASSIGNEE(S): OKI ELECTRIC IND CO LTD
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 11044443	A	19990216	Heisei	F24F007-06

APPLICATION INFORMATION

STN FORMAT: JP 1997-198682 19970724
 ORIGINAL: JP09198682 Heisei
 PRIORITY APPLN. INFO.: JP 1997-198682 19970724
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999

AN 1999-044443 JAPIO

AB PROBLEM TO BE SOLVED: To restrain the generation of low molecular siloxane(LMCS), generated from a seal member by a method wherein a fluorine base seal member is employed as a seal member employed for the constituting parts of a clean room itself.

SOLUTION: A gap between a HEPA filter 15 and the wall surface of a clean room 11 is sealed perfectly to isolate a clean room space 13 from a **plenum chamber** 17. A fluorine base seal member 18, produced by the polymer or the copolymer of vinylidene fluoride, hexafluoro propylene, tetrafluoro ethylene, perfluoro methyl vinyl ether and the like, for example, is employed for the seal member for the isolation. According to this method, LMCS, becoming contaminating gas for a semiconductor element, will not be generated and the adsorption of the LMCS to a member for semiconductor element is prevented whereby a uniform film, reduced in void, can be obtained upon forming a film, such as a gate oxidizing film, capacitor insulating film or the like.

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IC ICM F24F007-06

ICS H01L021-02; H01L021-027; H01L021-3065; H01L021-304; H01L021-31; H01L021-68

L169 ANSWER 6 OF 6 JAPIO COPYRIGHT 2002 JPO

ACCESSION NUMBER: 1983-124281 JAPIO
 TITLE: MANUFACTURE OF SOLAR BATTERY
 INVENTOR: OTAKE TSUTOMU
 PATENT ASSIGNEE(S): SEIKO EPSON CORP
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 58124281	A	19830723	Showa	H01L031-04

APPLICATION INFORMATION

STN FORMAT: JP 1982-7404 19820120
 ORIGINAL: JP57007404 Showa
 PRIORITY APPLN. INFO.: JP 1982-7404 19820120
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined

Applications, Vol. 1983

AN 1983-124281 JAPIO

AB PURPOSE: To improve the performance of the solar battery, by continuously changing the doping amount of boron without changing a total gas flow rate, thereby giving a gradient to the impurity concentration in a P layer.

CONSTITUTION: The temperature in a water bath 21 is detected by a thermocouple 25. The signal is fed back, and the flow rates of warm water through an **inlet port** 22 and cold water through an **outlet port** 23 are **controlled**.

. Thus the **temperature** of boron tribromide ($\text{BBr}_{3\text{SB}}$) is kept at a specified temperature. When $\text{H}_{2\text{SB}}$ gas is flowed from a gas introducing pipe 27 and the $\text{H}_{2\text{SB}}$ gas is discharged from a discharge pipe 28, $\text{BBr}_{3\text{SB}}$ is included in the $\text{BBr}_{3\text{SB}}$. The amount of inclusion depends on the vapor pressure of $\text{BBr}_{3\text{SB}}$, and said amount is **controlled** by the **temperature** of the water bath. The discharged $\text{H}_{2\text{SB}}$ gas is introduced into a reacting **chamber** of a plasma CVD apparatus, and the plasma discharge is performed together with $\text{SiH}_{4\text{SB}}$ gas. Then an a-Si film including the boron is formed. When the temperature of the water bath is changed, the amount of the boron included in the a-Si is changed.

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IC ICM H01L031-04

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FILE LAST UPDATED: 01 OCT 2002 <20021001/UP>
MOST RECENT DERWENT UPDATE 200263 <200263/DW>
DERWENT WORLD PATENTS INDEX SUBSCRIBER FILE, COVERS 1963 TO DATE

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L170 ANSWER 1 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 2002-517294 [55] WPIX

DNN N2002-409249 DNC C2002-146397

TI Open button **liner** formation method for semiconductor devices, involves injecting precursor gas such as tungsten carbonyl in **CVD chamber** to deposit tungsten onto sidewalls of openings.

DC A85 L03 U11

IN CABRAL, C; HU, C; MALHOTRA, S G; MCFEELY, F R; ROSSNAGEL, S M;
SIMON, A H

PA (IBM) INT BUSINESS MACHINES CORP

CYC 1

PI US 6380075 B1 20020430 (200255)* 9p H01L021-4763

ADT US 6380075 B1 US 2000-676546 20000929

PRAI US 2000-676546 20000929

IC ICM H01L021-4763

AB US 6380075 B UPAB: 20020829

NOVELTY - Several openings (48) are formed in a dielectric layer formed over a substrate, to expose an underlying conductive layer. The substrate is positioned in a **CVD chamber** for heating it to a temperature of 350 deg. C. A precursor gas such as tungsten carbonyl is injected into the **chamber** at a partial pressure lesser than 10 mTorr to deposit tungsten onto sidewalls (46) of the openings.

DETAILED DESCRIPTION - The substrate is provided with a pre-processed silicon **wafer** that has silicon oxide, polyimide or silicon nitride layer. The substrate is heated to 400 deg. C before the deposition step, to form an open-bottom **liner** for a conductor in the substrate structure. The residual metal deposited is removed from the bottom of the openings. A copper seed layer is also deposited by PVD, **CVD**, electroless or electroplating and ionized-physical vapor deposition (I-PVD) technique with the kinetic energy of the copper set to 50 eV. An electrical contact is established by depositing a metal film of the same material as the metal seed layer, such that a bond strength of $(0.4 \mu\text{pam})^{1/2}$ is attained.

An INDEPENDENT CLAIM is included for through-plug formation method.

USE - For forming **opening bottom liner** for conductor in electronic substrate structure for through-plug formation (claimed) in semiconductor devices.

ADVANTAGE - The porous or the open-bottom between the conductive metal of opening are significantly devoid of the flux divergence, hence voiding phenomenon is reduced, resulting in the suppression of electromigration damage. The physical sputtering completely eliminates **liner** formation at the bottom.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged cross-sectional view of the dual-damascene interconnect structure. Sidewalls 46

Openings 48

Dwg.3/4

FS CPI EPI

FA AB; GI

MC CPI: A12-E07C; L04-C01B; L04-C10J

EPI: U11-C05C3; U11-C05D3; U11-C05G2C; U11-D03B2

PLE UPA 20020829

[1.1] 018; P1081-R F72 D01; P0077; H0293

[1.2] 018; ND01; Q9999 Q7476 Q7330; K9676-R; K9483-R; K9585 K9483

L170 ANSWER 2 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 2002-270748 [32] WPIX

DNN N2002-210723

TI **Semiconductor** substrate **processing** apparatus

used for fabrication of integrated circuits, has multipurpose **chamber** with two cylindrical regions each having substrate support and exhaust system, respectively.

DC U11 V05

IN BARNES, M; HELMSEN, J J; MOHN, J D
PA (MATE-N) APPLIED MATERIALS INC
CYC 27
PI EP 1170777 A2 20020109 (200232)* EN 18p H01J037-32
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK
NL PT RO SE SI TR

JP 2002075974 A 20020315 (200234) 13p H01L021-3065
ADT EP 1170777 A2 EP 2001-116404 20010706; JP 2002075974 A JP
2001-208119 20010709

PRAI US 2000-611817 20000707
IC ICM H01J037-32; H01L021-3065
ICS H01L021-205

AB EP 1170777 A UPAB: 20020521
NOVELTY - Two cylindrical regions (204A,204B) and side walls (204) extend between the cylindrical regions to form a **chamber** (202). A substrate support (216) is provided internally in the cylindrical region (204A) and exhaust system (210) connected to **chamber** outlet (208) is connected to the cylindrical region (204B).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Processing **chamber** configuring apparatus;

(b) **Chamber**

USE - Used for fabrication of integrated circuits.

ADVANTAGE - The multipurpose **chamber** provides uniform plasma confinement around a substrate arranged in the **chamber** for various processing conditions and also provides efficient and uniform exhaust for processing gas from the **chamber**.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of a multipurpose **chamber** having two piece liner.

Chamber 202

Side walls 204

Cylindrical regions 204A,204B

Chamber outlet 208

Exhaust system 210

Substrate support 216

Dwg.3/9

FS EPI

FA AB; GI

MC EPI: U11-C09B; U11-C09C; V05-F04D1; V05-F04G; V05-F05C

L170 ANSWER 3 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 2002-205014 [26] WPIX

DNN N2002-156009 DNC C2002-062827

TI Formation of semiconductor device e.g., high-speed integrated circuit comprises sequentially forming oxide layer, silicon nitride layer, silicon oxime coating, and photoresist mask on substrate.

DC L03 U11

IN BABCOCK, C P; BHAKTA, J D

PA (BABC-I) BABCOCK C P; (BHAK-I) BHAKTA J D

CYC 1

PI US 2002009845 A1 20020124 (200226)* 11p H01L021-8238

ADT US 2002009845 A1 US 1999-376059 19990817

PRAI US 1999-376059 19990817

IC ICM H01L021-8238

ICS H01L021-76

AB US2002009845 A UPAB: 20020424

NOVELTY - A semiconductor device is made by sequentially forming oxide layer, silicon nitride layer, silicon oxime coating, and photoresist mask on a substrate.

USE - For making a semiconductor device, particularly high-speed integrated circuits having submicron design features and high conductivity reliable interconnect structures.

ADVANTAGE - The method is simplified, efficient, and less costly. The silicon oxime layer prevents the formation of standing waves and the negative effects during photoresist patterning. The method provides a device with accurately formed field dielectric regions.

DESCRIPTION OF DRAWING(S) - The drawing shows cross-sectional view of an on-process semiconductor device.

Liner oxide 60

Dielectric material 70

Dwg.1E/1

TECH US 2002009845 A1UPTX: 20020424

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The silicon nitride and silicon oxime layers are deposited in the same **chamber**. A nitrogen-containing gas and dichlorosilane are introduced to a plasma **chamber** to form the silicon nitride layer. Source gases employing an excess amount of nitrogen gas, are introduced to form the silicon oxime layer. The photoresist mask is patterned to form openings. The openings are etched. The substrate is etched to form line openings having a width of 0.15-0.3 microns. Openings are formed in the photoresist mask, silicon oxime layer, silicon nitride layer, oxide layer, and substrate. The photoresist mask is removed. The substrate in the **openings** are **lined** with an oxide. The openings are filled and the **liner** oxide (60) is **lined** with a dielectric material (70). The dielectric material and silicon oxime layer are polished to form field oxide regions. A conductive gate is formed on the substrate, with a gate oxide layer in between them. Dielectric spacers are formed on sidewalls of the gate. Source/drain regions are formed on either side of the gate by implantation of impurities. Preferred Parameters: The silicon oxide layer is 100-200 Angstrom thick. The silicon nitride layer is 1200-2000 Angstrom thick. The silicon oxime layer is 100-600 Angstrom thick. The silicon oxime layer has an extinction coefficient of greater than 0.4, preferably 0.4-0.6. The ratio of nitrogen-containing gas to dichlorosilane is 1:2 - 1:10.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The oxide layer comprises silicon dioxide. The silicon nitride is stoichiometric silicon nitride (Si₃N₄).

FS CPI EPI
FA AB; GI
MC CPI: L04-C06A; L04-C12A; L04-C12B; L04-C12E
EPI: U11-C04A1H; U11-C04E1; U11-C08A2

L170 ANSWER 4 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 2002-177999 [23] WPIX
DNC C2002-054853
TI Dry-etching apparatus for manufacturing semiconductor device.
DC A88 U11
IN CHOI, U C; KIM, H D; LEE, S Y; PARK, J H
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001058665 A 20010706 (200223)* 1p H01L021-3065
ADT KR 2001058665 A KR 1999-66019 19991230
PRAI KR 1999-66019 19991230
IC ICM H01L021-3065
AB KR2001058665 A UPAB: 20020411
NOVELTY - A dry-etching apparatus is to remove particles generated during etching, thereby obtaining a smooth etching.

DETAILED DESCRIPTION - A processing **chamber**(20) is maintained in a state of vacuum. The processing **chamber** comprises a window plate(10a) and a turbo plate(10b). The window plate is to monitor an interior of the processing **chamber**. A **liner**(24) is fitted to a hole of the window plate. A reaction **chamber**(28) is positioned on the processing **chamber**. The reaction **chamber** comprises a gas distributor, an upper electrode and a heater. The gas distributor is to supply plasma for the etching. The **liner** comprises protrusion to be inserted into a hole formed on a plate of a dry-etching apparatus. By the bottom portion of the **liner**, an excessive insertion of the **liner** into the **hole** is prevented. The **liner** is made of an elastic PTFE (polytetrafluoroethylene). Thickness of the **liner** is preferably 1 millimeter.

Dwg.1/10

FS CPI EPI
FA AB; GI
MC CPI: A04-E08B; A12-H
EPI: U11-C07A1; U11-C09C

L170 ANSWER 5 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 2001-182289 [18] WPIX
DNN N2001-130151 DNC C2001-054246
TI Low pressure **chemical vapor deposition** apparatus for forming metal films on silicon wafers, includes gas flow restrictor for controlling gas flow between **two** ends of **liner** tube.
DC L03 U11
IN PSAUTE, J H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1

PI US 6194030 B1 20010227 (200118)* 7p C23C016-00
ADT US 6194030 B1 US 1999-271515 19990318
PRAI US 1999-271515 19990318
IC ICM C23C016-00
AB US 6194030 B UPAB: 20010402

NOVELTY - A low pressure **chemical vapor deposition** apparatus includes a gas flow restrictor for controlling flow of gas between **two** ends of **liner** tube. The restrictor has apertures, which provide collective flow area.

DETAILED DESCRIPTION - A low pressure **chemical vapor deposition (LPCVD)** apparatus (10): comprises a **liner** tube (50) having a first end (54), a second end (56), and an interior (68) for accommodating the substrates between two ends. A gas supply system (140) provides reactive gas to the interior at or near the first end. A gas exhaust system (160) is provided for exhausting gas emerging from the second end. It includes an exhaust conduit (166) downstream from the second end. The conduit has a longitudinal axis and a cross-sectional area transverse to the longitudinal axis. A gas flow restrictor (120) having apertures (130) is provided at the second end for controlling the flow of gas between the two ends. The apertures provide collective flow area through the restrictor.

USE - The **LPCVD** apparatus is used for depositing a thin film on surfaces of the substrates, e.g. semiconductor wafers. It can be used to form metal films (e.g., for wiring), semiconductor films (e.g., for doping to form active areas), and insulating films (e.g., for insulating metal wires) on silicon wafers during integrated circuit fabrication.

ADVANTAGE - The **LPCVD** apparatus controls the velocity of flowing gas, thus improving the thin film uniformity.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of the **LPCVD** apparatus.

LPCVD apparatus 10

Chamber 14

Two ends of the chamber 24, 30

Chamber wall 34

Liner tube 50

Liner tube first end 54

Liner tube second end 56

Liner tube wall 60

Interior 68

Connector wall 70

First and second cavity 84, 86

Holder 110

Gas flow restrictor 120

Outer edge 128

Apertures 130

Gas supply system 140

Flow controller 148

Gas exhaust system 160

Exhaust conduit 166

Dwg.1/3

TECH US 6194030 B1 UPTX: 20010402

TECHNOLOGY FOCUS - MECHANICAL ENGINEERING - Preferred Components:

The **liner** tube having a pressure of 100 mTorr to 100 Torr has a wall (60) that constitutes a **CVD** furnace. The restrictor includes an outer edge (128) with a lip, which closely engages the **liner** tube wall when the restrictor is placed on the second end. The gas supply system includes a flow controller (148) for measuring gas flow. The **LPCVD** apparatus further includes a **chamber** (14) surrounding the **liner** tube and having two ends (24, 30) and a **chamber** wall (34). A connector wall (70) between the **liner** tube and the **chamber** wall forms first and second cavity (84, 86). The first cavity is defined by the connector wall, **chamber** wall, **chamber** second end, and **liner** tube; while the second cavity is defined by connector wall, **chamber** wall, and **chamber** first end. A holder (110) holds the substrates within the interior. A stationary wafer support within the **liner** tube supports the substrates in a fixed position.

FS CPI EPI

FA AB; GI

MC CPI: L04-C18; L04-D01

EPI: U11-C09B

L170 ANSWER 6 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 2001-079402 [09] WPIX

DNN N2001-060425 DNC C2001-022684

TI Formation of conducting metal lines and interconnects in vias and trenches in the fabrication of integrated circuit devices by dual damascene process and etch back techniques of copper oxide.

DC L03 U11

IN ROY, S R

PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE; (CHAR-N) CHARTERED SEMICONDUCTOR MFG CO LTD

CYC 2

PI US 6150269 A 20001121 (200109)* 7p H01L021-44

SG 78325 A1 20010220 (200117) H01L021-306

ADT US 6150269 A US 1998-151953 19980911; SG 78325 A1 SG 1998-4986 19981125

PRAI US 1998-151953 19980911

IC ICM H01L021-306; H01L021-44

ICS H01L021-3213; H01L021-461; H01L021-465; H01L021-4763; H01L023-34; H01L023-48

AB US 6150269 A UPAB: 20010213

NOVELTY - Planarized structures of conducting metal lines and interconnects (studs) are formed in vias and trenches in the fabrication of integrated circuit devices by dual damascene process and etch back techniques of copper oxides using a combination of oxidation of copper and chemical/mass transport of the copper oxide by the action of acid.

DETAILED DESCRIPTION - Formation of planarized structures of

conducting metal lines and interconnects (studs) in vias and trenches in the fabrication of integrated circuit devices involves: providing a substrate (1) upon which insulating material is deposited; depositing a conducting barrier layer that conforms to the insulating material and to the via holes and trenches; depositing a conducting metal over the entire substrate filling the via holes and trenches; oxidizing the surface of the conducting metal layer (14) over the entire substrate using oxidizing agents to form a metal oxide layer (16); and chemically etching back the metal oxide layer. The insulating material (10) is patterned and etched to form via holes and trenches in a dual damascene process.

USE - The method is used for forming planarized structures of conducting metal lines and interconnects (studs) in vias and trenches in the fabrication of integrated circuit devices.

ADVANTAGE - The etch back process solves the copper dishing problem by planarizing the copper. Etch back rates can be high at high temperatures, and the surface of the substrate is kept clean and free of polishing scratches from chemical mechanical polishing (CMP). The process produces better uniformity across the substrate and better electrical performance due to the increased copper line cross-sectional area. It eliminates exposing the soft copper metal to abrasive slurries.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional representations of the etch-back step.

Substrate 1

Insulating layer 10

Trench **liner** 12

Conducting metal layer 14

Metal oxide layer 16

2, 3, 4/7

TECH US 6150269 A UPTX: 20010213

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: The oxidizing and the etching back of the conducting metal layer are performed simultaneously or sequentially until the etch back is completed. The thin films of tantalum (Ta) and tantalum nitride (TaN) are **deposited by chemical vapor**

deposition (CVD). Oxidation includes introducing oxygen and hydrochloric acid (HCl) gas, or pyrogenic water and HCl gas into the **reactor** to form copper oxide. Etching back involves the removal of the copper oxide by HCl acidic gas. The method may include providing a bath or spray/spin station, providing steam and/or deionized water to oxidize conducting copper metal forming copper oxide, providing dilute HCl (approximately 0.1 molar) for copper oxide removal and continuing until the conducting copper metal is planarized back to the conducting barrier layer, and providing a deionized water rinse in nitrogen gas (N₂) blow dry followed by a thin coating of benzo-triazol (BTA) or tetra-triazol (TTA) corrosion protecting material.

Preferred Materials: The insulating material includes silicon oxide, borophosphosilicate glass (BPSG), or BPSG type materials. The barrier layer is conducting Ta/TaN acting as a via **hole** and trench **liner** (12), or as an etch stop layer for the

etch back. The conducting metal layer is copper.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The dual damascene technique forms conductive contacts to semiconductor diffusions and interconnection wiring patterns in the fabrication of metal oxide semiconductor field effect transistors (MOSFET's) or to multi-level metal lines and interconnection wiring patterns in the fabrication of semiconductor devices.

FS CPI EPI

FA AB; GI

MC CPI: L04-C06; L04-C07; L04-C10; L04-C12; L04-C13A; L04-C13B

EPI: U11-C05D3; U11-C05G2C; U11-C07C2; U11-C07D3

L170 ANSWER 7 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 2000-126866 [11] WPIX

CR 2000-147285 [13]; 2001-431527 [46]; 2002-237789 [29]

DNN N2000-095596 DNC C2000-038742

TI Elastomeric joint assembly in a plasma reaction **chamber** for use in **semiconductor** substrate **processing**.

DC A35 A85 L03 U11

IN HUBACEK, J S; KENNEDY, W S; LILLELAND, J; MARASCHIN, R A

PA (LAMR-N) LAM RES CORP

CYC 86

PI WO 2000000999 A1 20000106 (200011)* EN 66p H01L021-00

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
MW NL OA PT SD SE SL SZ UG ZW

W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK
LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG
SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW

AU 9949636 A 20000117 (200026) H01L021-00

EP 1105917 A1 20010613 (200134) EN H01L021-00

R: DE ES FR GB IT NL

KR 2001053289 A 20010625 (200173) H01L021-3065

CN 1312954 A 20010912 (200202) H01L021-00

KR 2001071688 A 20010731 (200208) H01L021-205

JP 2002519863 W 20020702 (200246) 54p H01L021-3065

ADT WO 2000000999 A1 WO 1999-US14790 19990630; AU 9949636 A AU
1999-49636 19990630; EP 1105917 A1 EP 1999-933616 19990630, WO
1999-US14790 19990630; KR 2001053289 A KR 2000-715011 20001229; CN
1312954 A CN 1999-809612 19990630; KR 2001071688 A KR 2000-715010
20001229; JP 2002519863 W WO 1999-US14790 19990630, JP 2000-557492
19990630

FDT AU 9949636 A Based on WO 2000000999; EP 1105917 A1 Based on WO
2000000999; JP 2002519863 W Based on WO 2000000999

PRAI US 1998-107471 19980630

IC ICM H01L021-00; H01L021-205; H01L021-3065

ICS H01L021-31

AB WO 2000000999 A UPAB: 20020722

NOVELTY - An elastomeric joint assembly in a plasma reaction **chamber** comprises: (a) a first and second part having bonding surfaces and (b) an elastomeric joint (46) between the first and the second part. The elastomeric joint attaches the first part

to the second part so as to allow movement between the two parts during temperature cycling.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for: (A) an electrode assembly; (B) a method for manufacturing an electrode assembly; (C) a method of **processing** a **semiconductor** substrate; and (D) a plasma processing system comprising: (D1) a plasma processing **chamber** with an interior space bounded by a **chamber**; (D2) a substrate support; (D3) a gas supply for supplying process gas to the interior space; (D4) an energy source for energizing the process gas into a plasma state; and (D5) a **liner** comprising a **ceramic** member supported by a resilient support **chamber**. The electrode assembly comprises: (A1) a support member; (A2) an RF driven electrode; and (A3) an elastomeric joint (46) between the outer edge of the electrode (42) and the support member. The method of (B) includes: (B1) applying an elastomeric material to the mating surfaces of the support member and the RF driven electrode; (B2) forming an assembly of the support member and electrode; (B3) curing the elastomeric bonding material to form an elastomeric joint between the electrode and the support member.

USE - The invention is used in **semiconductor** substrate **processing**.

DESCRIPTION OF DRAWING(S) - The figure shows a side sectional view of a showerhead electrode assembly.

Electrode 42

Support ring 44

Elastomeric joint 46

Recess 48

Dwg.3/12

TECH WO 200000999 A1UPTX: 20000301

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The elastomeric joint comprises a catalyst-cured elastomer resin or a polymeric material that is compatible in vacuum environment and resistant to thermal gradation at a temperature up to 200 degreesC. It is located in a recess (48) of the first part. The recess has uniform depth and located between the walls of the support member. The elastomeric joint (46) also includes filler of electrically and/or thermally conductive particles, preferably a filler of wire mesh, woven or non-woven fabric and most preferably a filler of metal particles. The filler has a particle size of 0.7-2 mum and an average size of at least 5 times smaller than depth of the recess in the interface. The elastomeric joint (46) is provided between the mating surfaces of the first and second parts. The mating surfaces are contoured to provide interlocking and/or self-aligning arrangement. The first part comprises an electrode and the second part comprises a showerhead electrode (42) and a support member. The support member of the electrode assembly is removably attached to a **temperature-controlled** member and the support member comprises a support ring (44). The **temperature-controlled** member includes a gas passage for supplying process gas. The elastomeric bonding material has a viscosity sufficient to achieve self-leveling and spreading on

the mating surfaces. The ceramic member of the plasma processing system comprises one-piece **ceramic liner** or an assembly of ceramic tiles and metal backing members. The resilient support comprises a bendable metal frame which is supported by a thermally controlled member and an elastomeric joint (46) between the ceramic member and the inner frame member. The bendable metal frame is cylindrical and includes a continuous upper portion and segmented lower portion. The **liner** includes a **ceramic** plasma screen extending from the lower portion of the ceramic member. The plasma screen is attached to the resilient support member by the electrically conductive elastomeric joint. The plasma processing system also comprises a heater supported by the bendable metal frame. Preferred Method: The recess extends around the support member and the electrode is bonded to the support member by the elastomeric joint. The method of (B) also includes: (a) preparing the elastomeric bonding material by mixing at least two components of an elastomer with an optional electrically conductive filler; (b) densifying the elastomeric bonding material; (c) applying masking material to surfaces of the electrode and support member; (d) aligning the electrode and support ring in a fixture; (e) degassing the bonding material; (f) applying material to the mating surfaces or plasma treating the mating surfaces; (g) applying pressure to force the excess bonding material out of the interface between the electrode and the support ring; and (h) heating the assembly. The semiconductor substrate of method (C) comprises silicon wafer and the method also includes etching a dielectric or conductive material layer on the wafer. Preferred Composition: The elastomeric joint contains 45-55 vol.% of the conductive filler.

TECHNOLOGY FOCUS - POLYMERS - Preferred Component: The polymeric material contains polyamide, polyketone, polyetherketone, polyether sulfone, polyethylene terephthalate, fluoroethylene propylene copolymers, cellulose, triacetates or silicone.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The metal particles comprise aluminum or an aluminum alloy (preferably an aluminum silicon alloy). The electrode consists of single crystal or polycrystalline silicon or a silicon disk of uniform or non-uniform thickness and the support member comprises a graphite support ring. The ceramic member preferably comprises one-piece silicon carbide (SiC) **liner** or a number of SiC tiles. Preferred Composition: The aluminum silicon alloy contains 5-20 wt.% silicon.

FS CPI EPI

FA AB; GI

MC CPI: A12-E; A12-H08; L03-H04D; L04-D04; L04-D10

EPI: U11-C09C

PLE UPA 20020508

[1.1] 018; P0635-R F70 D01

[1.2] 018; P1014-R P0964 P1149 H0260 F23 F34 D01; P1149-R F23 D01

- [1.3] 018; P1047 P0964 P1490 H0260 F34 F61 D01
- [1.4] 018; P0884 P1978 P0839 H0293 F41 D01 D11 D10 D19 D18 D31
D50 D63 D90 E21 E00
- [1.5] 018; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A;
R00976 G0022 D01 D12 D10 D51 D53 D59 D69 D83 F- 7A; H0022
H0011; P0544
- [1.6] 018; R01852-R G3634 D01 D03 D11 D10 D23 D22 D31 D42 D50
D76 D86 F24 F29 F26 F34 H0293 P0599 G3623; R17002 R01853
G3645 G3634 G3623 D01 D03 D11 D10 D23 D22 D31 D42 D50 D63
D76 D92 F24 F34 F41 F91 H0293 P0599
- [1.7] 018; P1445-R F81 Si 4A
- [1.8] 018; H0124-R; M9999 M2073; L9999 L2391; L9999 L2073
- [1.9] 018; ND01; K9449; K9949; K9427; Q9999 Q9018; Q9999 Q7498
Q7330; B9999 B3269 B3190; B9999 B4682 B4568; B9999 B3930-R
B3838 B3747
- [1.10] 018; D09 Gm Al 3A Si 4A; A999 A771; A999 A135; A999 A237;
S9999 S1514 S1456; B9999 B5527 B5505; B9999 B5209 B5185
B4740
- [1.11] 018; D09 Gm; A999 A135; A999 A237; A999 A760; B9999 B5527
B5505; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070
- [1.12] 018; A999 A157-R

L170 ANSWER 8 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1999-572222 [48] WPIX

DNN N1999-421659 DNC C1999-167115

TI Readily cleaned **chamber** for **chemical**
vapor deposition with reduced contamination.

DC L03 U11

IN BANG, W B; PHAM, T; YIEH, E

PA (MATE-N) APPLIED MATERIALS INC

CYC 21

PI WO 9949102 A1 19990930 (199948)* EN 29p C23C016-44
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR

US 6117244 A 20000912 (200046) C23C016-00

EP 1068371 A1 20010117 (200105) EN C23C016-44

R: BE DE IE NL

ADT WO 9949102 A1 WO 1999-US6485 19990324; US 6117244 A US 1998-47284
19980324; EP 1068371 A1 EP 1999-912884 19990324, WO 1999-US6485
19990324

FDT EP 1068371 A1 Based on WO 9949102

PRAI US 1998-47284 19980324

IC ICM C23C016-00; C23C016-44

AB WO 9949102 A UPAB: 19991122

NOVELTY - The **chamber** incorporates a **first**
ceramic **liner** adjacent to the substrate support to protect
the **chamber** wall, and a **second** ceramic
liner located in the pumping channel at the periphery of the
chamber to protect that channel. The ceramic is more
resistant to deposition and more readily cleaned than is aluminum.

DETAILED DESCRIPTION - Preferred Features: The ceramic
liners include aluminum oxide or nitride. There is a third

similar ceramic **liner** mounted on the periphery of the faceplate of the lid.

An INDEPENDENT CLAIM is also included for a **chemical vapor deposition reactor** system which includes a substrate heater and provision for supplying reagent gases into a mixing **chamber** to create a process gas. The gas distribution system, the substrate heater, and the vacuum system are controlled by a computer readable medium of a memory.

USE - Vacuum processing **chambers** for **processing semiconductor wafers**.

ADVANTAGE - Contamination of the substrate surface is reduced. Reduced cleaning time.

Dwg.0/5

FS CPI EPI
FA AB
MC CPI: L04-D01
EPI: U11-C09B; U11-C09F
DRN 1544-U

L170 ANSWER 9 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1999-204816 [17] WPIX

CR 2000-183323 [16]

DNN N1999-150881

TI Stable processing power for plasma **reactor**.

DC U11 V05

IN HWANG, J H; MAK, S S Y; YE, Y

PA (MATE-N) APPLIED MATERIALS INC

CYC 2

PI WO 9910913 A1 19990304 (199917)* EN 91p H01J037-32
W: JP

US 6277251 B1 20010821 (200150) C23C014-34

JP 2001514444 W 20010911 (200167) 80p H01L021-3065

ADT WO 9910913 A1 WO 1998-US16903 19980814; US 6277251 B1 Cont of US
1997-920283 19970826, US 2000-515695 20000229; JP 2001514444 W WO
1998-US16903 19980814, JP 2000-508131 19980814

FDT JP 2001514444 W Based on WO 9910913

PRAI US 1997-920283 19970826; US 2000-515695 20000229

IC ICM C23C014-34; H01J037-32; H01L021-3065

ICS C03C015-00; C23C014-54; C23C016-00; C23C016-505

AB WO 9910913 A UPAB: 20020117

NOVELTY - The plasma **reactor** has a **chamber** (102) containing a high density plasma (104) and a grounded cylindrical sidewall (108) with a dielectric ceiling (110). A pedestal (114) supports the **wafer** being **processed** in the center of the **chamber**. Uniformity of plasma distribution across the wafer is improved by shaping the ceiling (110) in a multi-radius dome. A **perforated liner** (11) supports assemblies (4) that receive the electrically conductive deposit and keep the inside surface of the ceiling window (110) free of deposit.

USE - Processing of **semiconductor wafers**

ADVANTAGE - Provides uniform processing over a long period of time

DESCRIPTION OF DRAWING(S) - - DESCRIPTION OF DRAWING -
Sectional view of plasma reactor.
deposit collectors 4

liner 11

chamber 102

plasma 104

sidewall 108

ceiling window 110

Dwg.14B/28

FS EPI

FA AB; GI

MC EPI: U11-C09C; V05-F05C1; V05-F08D1; V05-F08E1

L170 ANSWER 10 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1998-610399 [51] WPIX

DNC C1998-183084

TI Vertical furnace for treating semiconductor
substrates under reduced pressure - comprises heat treatment
chamber, 1st and 2nd chambers, and nozzles.

DC L03 U11

IN BUIJZE, J P; DE RIDDER, C G M; STOHR, H J J; STOUTJESDIJK, J J

PA (ASMI-N) ASM INT NV; (ADSE-N) ADVANCED SEMICONDUCTOR MATERIALS

CYC 82

PI WO 9850606 A1 19981112 (199851)* EN 14p C30B025-08

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC

MW NL OA PT SD SE SZ UG ZW

W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI

GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT

LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL

TJ TM TR TT UA UG US UZ VN YU ZW

NL 1005963 C2 19981109 (199908) C30B025-08

AU 9874567 A 19981127 (199915) C30B025-08

JP 2000513878 W 20001017 (200056) 16p H01L021-324

US 6225602 B1 20010501 (200126) F27B005-14

ADT WO 9850606 A1 WO 1998-NL246 19980505; NL 1005963 C2 NL 1997-1005963

19970502; AU 9874567 A AU 1998-74567 19980505; JP 2000513878 W JP

1998-547935 19980505, WO 1998-NL246 19980505; US 6225602 B1 WO

1998-NL246 19980505, US 1998-214446 19981229

FDT AU 9874567 A Based on WO 9850606; JP 2000513878 W Based on WO

9850606; US 6225602 B1 Based on WO 9850606

PRAI NL 1997-1005963 19970502

IC ICM C30B025-08; F27B005-14; H01L021-324

ICS C23C016-44; C30B031-10; H01L021-22; H01L021-68

AB WO 9850606 A UPAB: 19990107

A vertical furnace (1) for the treatment of semiconductor substrates

(20) under reduced pressure, comprises a treatment chamber

(7) limited by a 1st liner (13) of a refractory

material, around which is a 2nd liner (12) of a

quartz material arranged concentrically, and where a heating (11) is

arranged outside the 2nd liner when the heating

element is enclosed by refractory materials (10). The 1st liner (13) comprises SiC and is fitted to be stationary, and 1st and 2nd liners have 1st and 2nd nozzles at the top, where the 2nd nozzle is arranged concentrically around the 1st nozzle. The free end of at least one nozzle is connected to the remainder of the furnace via sealing means (21) which permit movement where the gap between 1st and 2nd liner can be put under reduced pressure and the 2nd liner is sealed relative to the surroundings.

USE - Furnace for treatment of semiconductor substrates.

ADVANTAGE - The furnace can be cleaned more easily and the operating period between two maintenance periods can be extended, so that the liner has a longer service life.

Dwg.1/2

FS CPI EPI
FA AB; GI
MC CPI: L04-D05
EPI: U11-C03A

L170 ANSWER 11 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1998-390840 [34] WPIX

DNN N1998-304993

TI Surface cleaning apparatus for CVD, PVD, etching apparatus
- includes temperature controller
controls temperature of liner so that
removal of sediment from liner is promoted.

DC U11

IN REDEKER, F C; STEGER, R J

PA (MATE-N) APPLIED MATERIALS INC

CYC 2

PI JP 10070112 A 19980310 (199834)* 12p H01L021-31

US 5788799 A 19980804 (199838) H01L021-00

ADT JP 10070112 A JP 1997-153946 19970611; US 5788799 A US 1996-661842
19960611

PRAI US 1996-661842 19960611

IC ICM H01L021-00; H01L021-31

ICS H01L021-02; H01L021-203; H01L021-205; H01L021-3065

AB JP 10070112 A UPAB: 19980826

The apparatus has a temperature controller
adjoined with surface of a processing chamber (100). The
controller controls the temperature of a
ceramic liner (102). Sediment formation on the
ceramic liner, during semiconductor
substrate processing is minimised.

ADVANTAGE - Prevents contamination of semiconductor with
sediments at high precision.

Dwg.1/4

FS EPI
FA AB; GI
MC EPI: U11-C09A; U11-C09B; U11-C09F

L170 ANSWER 12 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1998-065317 [07] WPIX

CR 2000-085322 [05]; 2001-030841 [64]; 2002-218829 [13]

DNN N1998-051336 DNC C1998-022775

TI **Chemical vapour deposition**

chamber - which includes a peripheral ring on the substrate support pedestal which is thermally insulated from the pedestal and the substrate..

AW **CVD**.

DC L03 U11

IN CHANG, M; DANEK, M; DORNFEST, C; LUO, L; SAJOTO, T; SCHRIEBER, A; SINHA, A; TEPMAN, A; WOLFF, S; ZHAO, J; SCHREIBER, A; ZHAO,

PA (MATE-N) APPLIED MATERIALS INC; (CHAN-I) CHANG M; (DANE-I) DANEK M; (DORN-I) DORNFEST C; (LUOL-I) LUO L; (SAJO-I) SAJOTO T; (SCHR-I) SCHREIBER A; (SINH-I) SINHA A; (TEPM-I) TEPMAN A; (WOLF-I) WOLFF S; (ZHAO-I) ZHAO

CYC 22

PI EP 818558 A1 19980114 (199807)* EN 28p C23C016-00
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

JP 10070088 A 19980310 (199820) 17p H01L021-285

US 5846332 A 19981208 (199905)

KR 98009511 A 19980430 (199915)

C23C016-44

US 5964947 A 19991012 (199949)

TW 359853 A 19990601 (200026)

H01L021-00

US 2001004478 A1 20010621 (200137)

C23C016-50

US 6270859 B2 20010807 (200147)

C23C016-34

EP 818558 B1 20020313 (200219) EN

C23C016-00

R: DE GB

DE 69710961 E 20020418 (200234) C23C016-00

ADT EP 818558 A1 EP 1997-305148 19970711; JP 10070088 A JP 1997-188357 19970714; US 5846332 A US 1996-680724 19960712; KR 98009511 A KR 1997-32160 19970711; US 5964947 A Div ex US 1996-680724 19960712, US 1997-857847 19970516; TW 359853 A TW 1997-108109 19970612; US 2001004478 A1 Div ex US 1996-680724 19960712, US 1998-49856 19980327; US 6270859 B2 Div ex US 1996-680724 19960712, US 1998-49856 19980327; EP 818558 B1 EP 1997-305148 19970711, Related to EP 2001-118816 19970711; DE 69710961 E DE 1997-610961 19970711, EP 1997-305148 19970711

FDT US 5964947 A Div ex US 5846332; US 2001004478 A1 Div ex US 5846332; US 6270859 B2 Div ex US 5846332; EP 818558 B1 Related to EP 1172458; DE 69710961 E Based on EP 818558

PRAI US 1996-680724 19960712; US 1997-857847 19970516; US 1998-49856 19980327

IC ICM C23C016-00; C23C016-34; C23C016-44; C23C016-50; H01L021-00; H01L021-285

ICS C23C016-14; H01L021-205

AB EP 818558 A UPAB: 20020528

A plasma **reactor** has a main processing **chamber** which includes a pedestal for supporting a substrate. A source of processing gas is disposed above the pedestal. A pumping channel surrounds a periphery of the **chamber** and is provided with

at least one removable **liner** placed on its walls. The channel is connected to the **chamber** by a passageway and is connectable to a vacuum pumping system. Also claimed is a substrate processing **reactor** with a reaction **chamber** which includes a pedestal for supporting a substrate to be processed. A source of gas is disposed over the pedestal and an exhaust valve is disposed around the pedestal on the sides of the **chamber**. A peripheral member is supported on the pedestal and thermally floats from the pedestal. Also claimed is a method of forming two **chemical vapour deposition (CVD)**

) layers on a substrate disposed in a reaction **chamber**. The method involves (i) supporting the substrate on a pedestal within a peripheral ring disposed on an upper periphery of the pedestal and having reduced thermal conduction between the ring and the pedestal, (ii) jetting a first reaction gas (g1) to the substrate from a perforated plate disposed in opposition to the substrate, (iii) exhausting (g1) from the space above the pedestal radially outward over the substrate and over the peripheral ring toward an annular pumping channel, (iv) heating the pedestal to a first processing temperature to cause (g1) to react with a surface of the substrate and deposit a film (f1) on it, (v) jetting a second reaction gas (g2) to the substrate from the perforated plate, (vi) exhausting (g2) from the reaction space radially outwardly over the substrate and over the ring toward the annular pumping channel and (vii) discharging (g2) in the reaction space into a plasma to react with the surface of the substrate to deposit a second film (f2) on it. At least one of f1 or f2 is conductive. Also claimed is a method of **CVD** depositing a film which involves (xi) depositing a film comprising titanium nitride on a substrate supported on a pedestal electrode within a reaction **chamber** and (xii) applying radio frequency (RF) power to a counter electrode while the pedestal electrode is RF grounded to form a plasma to treat the film. Also claimed is an isolator ring usable in a plasma reaction **chamber** comprising an electrically insulating ceramic material having a cylindrical shape. A first rim portion of the cylinder extends radially outward and a second skirt portion extends axially downward. Circumferential grooves are provided on a radially outwardly facing surface at a bottom of the skirt portion. Also claimed is a set of channel **liners** made of metals. The **liners** are a (1) a **first channel liner** shaped in a band, (2) a **second channel liner** shaped in a band having a greater diameter than (1), (3) a third channel **liner** having a radially extending portion extending between the first and second diameters and (4) an axially extending portion connected to (3) and having the diameter of (2). a peripheral ring on the substrate support pedestal which is thermally isolated from the pedestal and the substrate

USE - The apparatus is used in the manufacture of semiconductors.

ADVANTAGE - Plasma instability and arcing are reduced as is excessive build up on the portion of the susceptor extending beyond the edge of the substrate. Performance is improved by reducing the

formation of a continuous conductive film across the insulating elements within the **chamber**.

Dwg.8/21

FS CPI EPI
FA AB; GI
MC CPI: L04-D01
EPI: U11-C09B

L170 ANSWER 13 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1997-322161 [30] WPIX

CR 1996-261632 [27]; 2000-595693 [57]; 2000-640221 [62]

DNC C1997-104260

TI **Ceramic liner** reducing residues in a plasma-processing **chamber** - especially around the exhaust **outlet**, including an air gap between the **liner** and the **chamber** walls which increases the dielectric value of the **ceramic liner**.

DC L03 P78

IN CHO, T; GUO, X S; JUN, Z; QIAO, J; SCHREIBER, A; TABATA, A; ZHAO,

PA (MATE-N) APPLIED MATERIALS INC

CYC 5

PI EP 780490 A1 19970625 (199730)* EN 14p C23C016-44

R: DE GB

JP 09251992 A 19970922 (199748) 11p H01L021-31

KR 97051833 A 19970729 (199910) H01L021-02

US 5885356 A 19990323 (199919) C23C016-00

EP 780490 B1 20000614 (200033) EN C23C016-44

R: DE GB

DE 69608873 E 20000720 (200041) C23C016-44

KR 284571 B 20010402 (200216) H01L021-02

ADT EP 780490 A1 EP 1996-309217 19961217; JP 09251992 A JP 1996-335940 19961216; KR 97051833 A KR 1996-71125 19961221; US 5885356 A CIP of US 1994-348273 19941130, US 1995-577862 19951222; EP 780490 B1 EP 1996-309217 19961217; DE 69608873 E DE 1996-608873 19961217, EP 1996-309217 19961217; KR 284571 B KR 1996-71125 19961221

FDT US 5885356 A CIP of US 5558717; DE 69608873 E Based on EP 780490; KR 284571 B Previous Publ. KR 97051833

PRAI US 1995-577862 19951222; US 1994-348273 19941130

REP 2.Jnl.Ref; EP 463633; JP 05055184; JP 59023520; US 5269881; US 5304279; US 5366585

IC ICM C23C016-00; C23C016-44; H01L021-02; H01L021-31

ICS B44C001-22; C23C016-50; C30B025-14; H01L021-205

AB EP 780490 A UPAB: 20020308

A processing apparatus for applying a material to a substrate comprises: a) a processing **chamber** for enclosing the substrate; b) an **inlet** (14) for introducing the processing material; c) an exhaust **outlet** (24,222) for removal of processing material; and d) a ceramic layer (30,32) covering a portion of the exhaust **outlet**. A processing apparatus as above including an air gap between the majority of the ceramic layer and the electrically conductive portion of the **chamber**. A processing apparatus as above in which the ceramic layer is attached

to the walls of the **chamber** by a securing member which is electrically insulating. A method for cleaning a processing **chamber** used for applying a material to a substrate by creating a plasma with an electric field, wherein a cleaning gas is introduced into the **chamber** whilst the ceramic layer still retains heat from a previous processing step. A processing apparatus for plasma-enhanced **chemical vapour deposition** (PECVD) as above which includes a pedestal (10) for supporting the substrate, the gas distribution manifold and the pedestal being electrically charged to impose a voltage potential between them, and the processing **chamber** being provided with an electrical ground. A **first ceramic liner** covers a portion of the exhaust **outlet** which is electrically grounded and a **second ceramic liner** lines an inside portion of the **chamber**.

USE - Useful in the field of **semiconductor processing**, especially for reducing the residues in a plasma processing **chamber**.

ADVANTAGE - The use of a **ceramic liner** reduces the accretion of deposits on **chamber** walls and around the exhaust areas of a plasma-processing **chamber**. An air gap between the **ceramic liner** and the processing **chamber** walls increases the dielectric value of the **ceramic liner**, and allows it to retain sufficient heat to eliminate the need for the heaters typically used to heat the aluminium walls during the **chamber**-cleaning.

Dwg.2/6

FS CPI GMPI
FA AB; GI
MC CPI: L04-D

L170 ANSWER 14 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1993-074357 [09] WPIX

DNC C1993-033065

TI Chemical processes activator - has rotating discs with arc-shaped ferromagnetic elements, vibrated by opposing magnets, located respectively above and below disc.

DC J02

IN ZELTSER, P YA

PA (ESIG-R) E SIBE GEOL GEOPHYS & MINERALS RES INST

CYC 1

PI SU 1722559 A1 19920330 (199309)* 3p B01F013-08

ADT SU 1722559 A1 SU 1988-4394090 19880216

PRAI SU 1988-4394090 19880216

IC ICM B01F013-08

AB SU 1722559 A UPAB: 19930924

The appts. has a working cylindrical **chamber** (1), delivery (7) and removal (8) pipes, rotating shaft (9) with discs (6) and electromagnets (4), fitted opposite each other in non-magnetic holders (5). The discs (6) have central openings (17) with conical sides (18), have rods (19) on their bottom surfaces and deflectors

(13), consisting of joined cylindrical rings (14) and perforated conical rings (15). Free to vibrate arc-shaped ferromagnetic elements (12) are fitted on periphery of the discs (6) and interact with magnetic fields of the electromagnets (4), displaced respectively above and below the disc (6).

USE/ADVANTAGE - In construction mainly for intensive activation of binding materials, e.g. of cement slurry used for **lining** drilled **holes**. Bul.12/30.3.92

1/3

FS CPI
FA AB; GI
MC CPI: J02-A02B

L170 ANSWER 15 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1992-034056 [05] WPIX

DNC C1992-014802

TI Varying the inner profile in a tubular co-extrusion process - has a variable inner die orifice through which the **liner** material is fed for tyre prodn..

DC A32

IN SICKA, R W; TOMPKINS, D A

PA (BRID) BRIDGESTONE FIRESTONE INC; (BRID) BRIDGESTONE CORP

CYC 7

PI EP 468261 A 19920129 (199205)*

R: DE ES FR GB IT

US 5128084 A 19920707 (199230) 17p B29C047-02

EP 468261 A3 19920429 (199329)

JP 06320597 A 19941122 (199506) 11p B29C047-06

EP 468261 B1 19950913 (199541) EN 21p B29C047-06

R: DE ES FR GB IT

DE 69112944 E 19951019 (199547) B29C047-06

ES 2076422 T3 19951101 (199550) B29C047-06

JP 2530396 B2 19960904 (199640) 11p B29C047-06

ADT EP 468261 A EP 1991-111301 19910706; US 5128084 A US 1990-558061 19900724; EP 468261 A3 EP 1991-111301 19910706; JP 06320597 A JP 1991-205715 19910723; EP 468261 B1 EP 1991-111301 19910706; DE 69112944 E DE 1991-612944 19910706; EP 1991-111301 19910706; ES 2076422 T3 EP 1991-111301 19910706; JP 2530396 B2 JP 1991-205715 19910723

FDT DE 69112944 E Based on EP 468261; ES 2076422 T3 Based on EP 468261; JP 2530396 B2 Previous Publ. JP 06320597

PRAI US 1990-558061 19900724

REP NoSR.Pub; DE 3301248; EP 158814; EP 254996; EP 359088; EP 370695; FR 2332121; GB 1456198; GB 2050933; US 4578024

IC ICM B29C047-02; B29C047-06

ICS B29C047-22; B29C047-26; B29C047-28

ICI B29K021:00, B29L009:00, B29L023:00, B29L030:

AB EP 468261 A UPAB: 19970502

Coextrusion appts. has means for varying the inner profile of a tubular extrudate which comprises an outer die assembly with an outer annular orifice formed between an outer die ring and an inner ring which is also a component of an inner die assembly. The inner

die assembly has an axially movable die ring which forms an adjustable inner extrusion orifice. A first stream of an elastomeric compound is fed to the outer orifice to form the tubular extrudate and a second stream of elastomeric material is fed to the inner orifice, thus depositing a layer of the second elastomeric compound onto the inner surface of the tubular extrudate. Means are provided to vary the flow of elastomeric material through inner orifice, by axial movement of die ring, with a cooperating axially movable compensating ring to control the pressure in the second elastomeric stream being deposited on the inner surface of the tubular extrusion.

The inner ring is pref. moved by a piston attached to it to adjust the size of the inner orifice. A second piston moves the compensating ring. The inner die ring is pref. axially downstream of the anvil ring, whilst the surfaces of the die ring, and anvil ring are arranged radially such that the second elastomeric stream moves in a generally radial direction when being deposited on the inner surface of the tubular extrudate.

USE/ADVANTAGE - Used for production of elastomeric annular seamless items, partic. for tyres and specifically for body plies for use in a first stage tyre. Enables the inner **liner** application to be started or stopped abruptly with no smearing or contamination. Reinforcing filaments or cords may be introduced into the composite during extrusion and with the simultaneous application of the **liner**. @(19pp Dwg.No.0/15)@

ABEQ US 5128084 A UPAB: 19931006

A coextrusion appts. for varying the inner profile of a tubular extrudate comprises an outer die assembly forming an outer annular extrusion orifice, an inner die assembly having an axially moveable die ring forming an adjustable inner extrusion orifice. A mechanism is provided for forming an outer tubular flow channel for delivering a first elastomer stream to the outer orifice of the outer assembly to form the extrudate.

A second mechanism is provided for forming an inner tubular flow channel for a second such stream to the inner assembly orifice for selective deposition of a layer on the extrudate inner surface. A further device for flow control of the second stream is provided for varying the extrudate profile. This device comprises a compensating ring movable only axially opposite the movement of the inner die to control flow press.

USE - For making tyre body profiles.

0/15

ABEQ EP 468261 B UPAB: 19951019

A coextrusion appts. for varying the inner profile of a generally tubular extrudate (82) during the formation of the extrudate, wherein the coextrusion appts. includes an outer die assembly (8) for forming an outer annular extrusion orifice (27) for forming the tubular extrudate, an inner die assembly (10) having an axially movable die ring (35) for forming an adjustable inner extrusion orifice (49), a first means (2,18,19) for forming an outer tubular flow channel (7A) for delivering a first stream (7) of elastomeric material to the outer extrusion orifice (27) of the outer die

assembly to form the tubular extrudate, and second means (2,18,19,20) for forming an inner tubular flow channel for delivering a second stream (6) of an elastomeric material to the inner extrusion orifice of the inner die assembly for selectively depositing a layer of the elastomeric material on an inner surface (81) of the tubular extrudate, and third means for controlling the flow of the second stream of elastomeric material through the inner orifice to change the amt. of the elastomeric material deposited on the inner surface of the tubular extrudate to vary the profile of the inner surface, characterised in that the third means including an axially movable compensating ring (40) cooperating with the axial movement of the inner die ring (35) for controlling the pressure within the second stream (6) of elastomeric material moving through the inner extrusion orifice (49) and being deposited on the inner surface (82) of the tubular extrudate and the third means further including a first fluid pressure actuated device (36) attached to the inner die ring (35) for axially moving the inner die ring for adjusting the size of an inner extrusion orifice (49) formed between the inner die ring (35) and an anvil ring (9), of the inner extension orifice (49) formed between the inner die ring (45) and the anvil ring (9), in that a second fluid pressure actuated device (38) is connected to the compensating ring (40) for axially moving the compensating ring in a direction opposite to the direction of movement of the inner die ring (35), in which the first (36) and second (38) fluid pressure actuated devices are first and second piston rods respectively, in that the inner die ring (35) is located concentrically about the compensating ring (40) and has an inner cylindrical surface (93) slidably engaged with a cylindrical outer surface (94) of the compensating ring in which the compensating ring (40) terminates in an annular inner end face (95) which forms an expansion chamber (85) in communication with the inner tubular flow channel, and in which the compensating ring (40) moves in an axial direction opposite to that of the inner die ring (35) to compensate for the pressure within the second stream (6) of elastomeric material caused by varying the size of the orifice (49) upon movement of the inner die ring.

Dwg.4/15

FS CPI

FA AB

MC CPI: A11-B07B; A12-T01A

PLC UPA 19930924

KS: 0009 0011 0223 0229 2212 2353 2356 2491 2654 2826 3234 3236

FG: *001* 014 03- 032 308 309 371 388 41& 415 450 46& 57& 575 59&
596 672 723

L170 ANSWER 16 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1991-065224 [09] WPIX

DNN N1991-050520

TI Reactant exhaust for thermal processing furnace - has scavenger to remove effluent reactant gases with radial flow.

DC Q77 U11

IN PHILIPPOSSI, A
 PA (DIGI) NIPPON DIGITAL EQUIP KK
 CYC 2
 PI US 4992044 A 19910212 (199109)*
 JP 03036719 A 19910218 (199113)
 ADT US 4992044 A US 1989-372663 19890628; JP 03036719 A JP 1990-171301
 19900628
 PRAI US 1989-372663 19890628
 IC F27D005-00; F27D007-02; H01L021-22
 AB US 4992044 A UPAB: 19930928
 The furnace, used for high-temp. **processing** of
semiconductor wafers, employs a scavenger
 arrangement for removing effluent reactant gases which provides
 radial symmetry of gas flow. A scavenger **chamber** surrounds
 one end of a cylindrical furnace, and draws exhaust gases outward by
 a pressure differential.
 The scavenger **chamber** has a cylindrical quartz
liner having **openings**. The openings are
 circumferentially spaced about the end of the furnace so that gas
 flow is uniform and symmetrical. These openings are in distributed
 groups.
 1/10
 FS EPI GMPI
 FA AB; GI
 MC EPI: U11-C03A

L170 ANSWER 17 OF 18 WPIX (C) 2002 THOMSON DERWENT
 AN 1990-060034 [09] WPIX
 DNN N1990-046140 DNC C1990-026064
 TI **Reactor** for gas phase deposition or etching - has inner
 wall provided with gas cushion to prevent unwanted precipitation
 deposits.
 DC L03 M14 P78 Q77 U11 X25
 IN FABIAN, L; MOLLER, R; RESCH, D
 PA (VMAT) VEB ELEKTROMAT DRESDEN
 CYC 6
 PI DE 3923538 A 19900222 (199009)*
 GB 2222182 A 19900228 (199009)
 FR 2635377 A 19900216 (199014)
 JP 02101169 A 19900412 (199021)
 DD 274830 A 19900103 (199024)
 US 4981722 A 19910101 (199104)
 GB 2222182 B 19921118 (199247) C23C016-00
 ADT DE 3923538 A DE 1989-3923538 19890715; GB 2222182 A GB 1989-17677
 19890802; FR 2635377 A FR 1989-10295 19890731; JP 02101169 A JP
 1989-198113 19890801; US 4981722 A US 1989-378533 19890711; GB
 2222182 B GB 1989-17677 19890802
 PRAI DD 1988-318880 19880812
 IC B44C001-22; C23C016-50; C23F004-00; F27B005-04; F27D001-12;
 F27D007-02; H01L021-20; H01L021-36
 AB DE 3923538 A UPAB: 19930928
 Gas phase **reactor** for working disc-shaped workpieces has

an outer wall (1) which is water cooled and as inner wall (8) which is spaced from the outer wall and provided with openings which allow the passage of a flushing gas blown into the **chamber** via conduits (9). The flushing gas is suction removed via suction canals (10) located away from the entry and exit conduits (11, 12) for the process gas.

USE/ADVANTAGE - **Chemical vapour deposition** a plasma chemical **etching** of **semi-conductor** substrates. The flow of flushing gas reduces the amount of precipitation deposits on the walls thereby increasing the time between cleaning of the **reactor**

ABEQ GB 2222182 B UPAB: 19930928

Equipment for the gas-phase **treatment** of **disc**-shaped workpieces, consisting of a cold-wall **reactor** having a water cooled outer, first wall system defining an interior of the **reactor**, said interior being **lined** with a gas-permeable second wall system which is arranged at a defined distance from the first wall system to define **plenums** for a flushing gas, the **lining** being located wherever the **reactor** parts are not required to be unlined, treatment gas inlet and outlet means for conducting into and out of the **reactor** a treatment gas for treating the work piece, the treatment gas outlet means being connected to a treatment gas extractor, flushing gas inlet means for conducting flushing gas into the **plenums** between the first and second wall systems, and flushing gas extraction channels being provided at locations where part surfaces of the gas-permeable second wall system abut to form a corner, the extraction channels being connected to a flushing gas extractor which is separate from the treatment gas extractor.

1/1

ABEQ US 4981722 A UPAB: 19930928

Disk-shaped semiconductor substrates are gas-phase processed in equipment having an external, water-cooled wall system (1), closed off by a HF electrode (2), also supplying (11) and exhausting (12) gas. Reaction space is closed off at the bottom by a radiation window (4), separating off the radiant heating system (5). Disk-shaped substrate is placed on a support (7), acting as ground electrode. A gas-permeable second wall system (8), spaced inside the first system, shields the latter completely. Gas inlets (9) and an exhaust system (10) for a flushing gas generate a gas cushion on the inner wall of the second system.

ADVANTAGE - Particle generation in the **chamber** is reduced, lengthening service life. @@

FS CPI EPI GMPI

FA AB

MC CPI: L04-C07B; L04-D01; M13-E07

EPI: U11-C01A9; U11-C01B; U11-C07A1; U11-C09B; U11-C09C; X25-A04

L170 ANSWER 18 OF 18 WPIX (C) 2002 THOMSON DERWENT

AN 1975-03177W [02] WPIX

TI Clay-like raw material **processing** - employing conical **discs** with **perforated lining** to improve grinding efficiency.

DC L02 P41

PA (FERR-N) FERROCONCRETE NO 3 WORKS

CYC 1

PI SU 417158 A 19740723 (197502)*

PRAI SU 1972-1789724 19720529

IC B02C007-12

AB SU 417158 A UPAB: 19930831

Improved efficiency of grinding and processing plastic materials, such as e.g. clayey raw materials, is ensured by mounting working conical discs so that they form a working **chamber** with space diminishing in the direction of turning, and covering them by a **perforated lining**. On stand the motors drive shafts mounted in bearing units at suitable angle to each other, with conical working units enclosed in cylindrical case. Working surfaces of cones, whose apexes are touching, are covered with **perforated linings**. The wall in case is also perforated. The working cones are pressed to each other by springs backed by adjustable discs. The raw materials is loaded into hopper and the processed material is discharged by chute. During processing, part of the material passes through the **perforations** in **linings** and another part, carried into the gap between the discs, forming due to the tension of springs, returns for reprocessing.

FS CPI GMPI

FA AB

MC CPI: L02-A02; L02-A03

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L174 ANSWER 1 OF 19 HCA COPYRIGHT 2002 ACS

137:14304 **Semiconductor-processing chamber**

having **temperature-controlled liners**

equipped for fluid flow. Noorbakhsh, Hamid; Salimian, Siamak; Luscher, Paul; Carducci, James D.; Lee, Evans; Vaidya, Kaushik; Shan, Hongqing; Welch, Michael D. (Applied Materials, Inc., USA). U.S. Pat. Appl. Publ. US 20020069970 A1 20020613, 17 pp., Division of U. S. Ser. No. 519,719. (English). CODEN: USXXCO. APPLICATION: US 2002-55310 20020122. PRIORITY: US 2000-519719 20000307.

AB The **chamber** app. for **semiconductor processing** is equipped with inner-wall **liner** having a fluid passage system for **temp. control**. The **chamber** wall is typically made of Al, stainless steel,

and/or ceramic materials. The inner **chamber** wall optionally includes the 1st and/or 2nd **liners**, esp. to maintain a predetd. **temp.** by **temp.-controlled** fluid flow through the passage system. The **chamber** operation with a predetd. **temp.** avoids deposition of films on the **chamber liner**, as well as particle generation due to stress cracking of deposited films.

- IC ICM C23F001-02
ICS C23C016-00
- NCL 156345370
- CC 76-2 (Electric Phenomena)
- ST **semiconductor processing hot chamber**
wall cooling fluid flow
- IT Process control
(**chamber app.**; **semiconductor-**
processing chamber having **temp.-**
controlled liners with fluid flow)
- IT **Linings** (nonrefractory)
(**chamber-app.**; **semiconductor-**
processing chamber having **temp.-**
controlled liners with fluid flow)
- IT **Ceramics**
Cooling apparatus
(**linings, chamber app.** with;
semiconductor-processing chamber
having **temp.-controlled liners** with
fluid flow)
- IT **Semiconductor materials**
(**processing of; semiconductor-**
processing chamber having **temp.-**
controlled liners with fluid flow)
- IT 7429-90-5, Aluminum, uses 12597-68-1, Stainless steel, uses
(wall, **chamber app.** with; **semiconductor-**
processing chamber having **temp.-**
controlled liners with fluid flow)

L174 ANSWER 2 OF 19 HCA COPYRIGHT 2002 ACS

136:255630 Quartz-lined **chamber** for clean
high-temperature **processing** of **semiconductor**
wafers. Raaijmakers, Ivo (USA). U.S. Pat. Appl. Publ. US
20020033232 A1 20020321, 19 pp., Cont.-in-part of U. S. Ser. No.
394,372. (English). CODEN: USXXCO. APPLICATION: US 2001-995323
20011126. PRIORITY: US 1999-394372 19990910.

- AB A process **chamber app.** having top-dome shape and circular
structure is **lined** on the interior surface with quartz for
a clean finish, and is equipped with **inlet** and
outlet flanges for attachable door units and gas-flow
connections. The upper, lower, and side walls enclose an all-quartz
interior surface, except for the loading connections. An internal
reinforcement extends along the **chamber** perimeter to
provide addnl. strength and support, and an external reinforcement
surrounds the cylindrical side wall to confine outward expansion of

the **chamber**. The **chamber** is typically equipped with internal susceptor unit for induction heating with **temp control**, and is suitable for high-temp. **processing of semiconductor wafers** with a gas flow. The **chamber** is optionally designed with the upper and lower dome walls having rectangular plan when viewed from above, and typically has the length of 600 mm, width of 300 mm, and internal height of 50 mm to **process a wafer** having 200 mm size.

- IC ICM C23F001-02
- ICS C23C016-00
- NCL 156345000
- CC 76-2 (Electric Phenomena)
- Section cross-reference(s): 47
- ST **semiconductor hot processing chamber**
- quartz internal lining
- IT **Containers**
- (**chamber** app.; quartz-lined **chamber** for clean high-temp. **processing of semiconductor wafers**)
- IT Electric furnaces
- (induction, susceptor for, **chamber** app. with; quartz-lined **chamber** for clean high-temp. **processing of semiconductor wafers**)
- IT **Semiconductor materials**
- (**wafers, processing of; quartz-lined chamber** for clean high-temp. **processing of semiconductor wafers**)
- IT 14808-60-7, Quartz, uses
- (**lining, chamber** with; quartz-lined **chamber** for clean high-temp. **processing of semiconductor wafers**)

L174 ANSWER 3 OF 19 HCA COPYRIGHT 2002 ACS

136:225377 **Chamber** of a device for quickly and economically producing a semiconductor device. Bae, Gyeong Jeong; Son, Gwon (Samsung Electronics Co, Ltd., S. Korea). Repub. Korean Kongkae Taeho Kongbo KR 2000050503 A 20000805, No pp. given (Korean). CODEN: KRXXA7. APPLICATION: KR 1999-427 19990111.

- AB A **chamber** of a device for producing a semiconductor device saves costs and hours by sepg. a dividing member placed on an opening from a body to replace only an etched divided member. A **chamber** comprises: a body having an inside space and an opening on its one side; a **liner** having an **opening** corresponding to the opening of the body; and a divided member arranged on the opening and engaged with the body. When the **chamber** is required, only the divided member is replaced. A device for producing the **semiconductor** comprises: a **process chamber** having an inner space, an opening on its one surface and an anodization film applied on its wall surface; a buffer **chamber** having an opening corresponding to the opening of the process **chamber** and moving a

wafer to the process chamber; a liner for protecting the anodization film of the process chamber; and a slit valve having one end supported at inside of the process chamber and another end projected out of the process chamber to be connected to the buffer chamber to accomplish an insertion and withdrawal of the wafer.

- IC ICM H01L021-20
- CC 76-3 (Electric Phenomena)
- ST **chamber** valve anodization **etching**
semiconductor device fabrication
- IT Semiconductor device fabrication
(app.; **chamber** of device for quickly and economically producing semiconductor device)
- IT Anodization
Etching
(**chamber** of device for quickly and economically producing semiconductor device)
- IT Valves
(slit; **chamber** of device for quickly and economically producing semiconductor device)

L174 ANSWER 4 OF 19 HCA COPYRIGHT 2002 ACS

134:246042 **Semiconductor processing** equipment having radiant heated **ceramic liner**. Kennedy, William S.; Maraschin, Robert A.; Wicker, Thomas E. (Lam Research Corporation, USA). PCT Int. Appl. WO 2001022478 A1 20010329, 25 pp. DESIGNATED STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG. (English). CODEN: PIXXD2. APPLICATION: WO 2000-US24866 20000911. PRIORITY: US 1999-401308 19990923.

- AB A plasma processing **chamber** including a **ceramic liner** heated by radiant heating. The **liner** can be tiles or a continuous cylindrical **liner**. The **liner** and other parts such as a gas distribution plate and a plasma screen can be made of SiC which advantageously confines the plasma and provides **temp. control** of the inner surfaces of the **chamber**. To remove excess heat from the **liner**, the **ceramic liner** can be supported on a resilient Al support frame which conducts heat from the **liner** to a **temp. controlled** member such as a top plate of the **chamber**. The support frame can include a continuous upper portion and a segmented lower portion which allows thermal stresses to be accommodated during **processing** of **semiconductor** substrates in the plasma chamber.

IC ICM H01L021-00
 CC 76-2 (Electric Phenomena)
 Section cross-reference(s): 57
 ST **semiconductor processing** equipment radiant
 heated **ceramic liner**
 IT Tiles
 (ceramic; **semiconductor processing** equipment
 having radiant heated **liner**)
 IT Plasma
 (processing **chamber** having radiant heated
ceramic liner for semiconductor equipment)
 IT **Semiconductor** materials
 (processing equipment having radiant heated
ceramic liner)
 IT Radiative heat transfer
 (**semiconductor processing** equipment having
ceramic liner with **aluminum** support
 frame for)
 IT **Linings** (refractory)
 (**semiconductor processing** equipment having
 radiant heated **ceramic liner**)
 IT Ceramics
 (**semiconductor processing** equipment having
 radiant heated **liner**)
 IT 7429-90-5, Aluminum, uses
 (**semiconductor processing** equipment having
 radiant heated **ceramic liner** by support frame
 of)
 IT 409-21-2, Silicon monocarbide, uses
 (**semiconductor processing** equipment having
 radiant heated **liner**)

L174 ANSWER 5 OF 19 HCA COPYRIGHT 2002 ACS

134:246041 **Semiconductor processing** equipment having
 tiled **ceramic liner**. Kennedy, William S.;

Maraschin, Robert A.; Hubacek, Jerome S. (Lam Research Corporation,
 USA). PCT Int. Appl. WO 2001022471 A1 20010329, 30 pp. DESIGNATED
 STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA,
 CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM,
 HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT,
 LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD,
 SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA,
 ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG,
 CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML,
 MR, NE, NL, PT, SE, SN, TD, TG. (English). CODEN: PIXXD2.

APPLICATION: WO 2000-US24868 20000911. PRIORITY: US 1999-401193
 19990923.

AB A plasma processing **chamber** including a **ceramic**
liner as **ceramic** tiles mounted on a resilient
 support member. The **liner** and other parts such as a gas
 distribution plate and a plasma screen can be made of SiC which
 advantageously confines the plasma and provides temp.

control of the inner surfaces of the chamber. The liner can be heated by a heater which provides heat to the liner by thermal conduction. To remove excess heat from the liner, the resilient support can be an Al support frame which conducts heat from the liner to a temp.

controlled member such as a top plate of the chamber

. The support frame can include a continuous upper portion and a segmented lower portion which allows thermal stresses to be accommodated during processing of semiconductor substrates in the plasma chamber.

- IC ICM H01J037-32
- ICS C23C016-50
- CC 76-2 (Electric Phenomena)
- Section cross-reference(s): 57
- ST semiconductor processing equipment tiled ceramic liner
- IT Tiles
(ceramic; semiconductor processing equipment having liner of)
- IT Semiconductor materials
(processing equipment having tiled ceramic liner)
- IT Ceramics
(semiconductor processing equipment having liner of tiled)
- IT Linings (refractory)
(semiconductor processing equipment having tiled ceramic)
- IT Radiative heat transfer
(semiconductor processing equipment having tiled ceramic liner using aluminum support frame for)
- IT 409-21-2, Silicon monocarbide, uses
(semiconductor processing equipment having liner of tiled)
- IT 7429-90-5, Aluminum, uses
(semiconductor processing equipment having tiled ceramic liner on heat conducting support frame of)

L174 ANSWER 6 OF 19 HCA COPYRIGHT 2002 ACS

133:21606 Apparatus for decomposition of residual ozone from water treatment or semiconductor device cleaning.

Toyota, Kimiyoshi (Chlorine Engineers Corp., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2000167351 A2 20000620, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-366093 19981207.

- AB The app. comprises means for blowing upwardly gaseous effluents contg. residual O3 (esp. from water treatment or semiconductor device cleaning or paper pulp bleaching plants) through a fixed bed of catalyst-loaded activated carbon grains in a vertical cylindrical chamber having inlet at bottom and outlet at top, and means for

maintaining the catalyst bed temp. at 40-50.degree. by an indirect-contact cooling system having liq. or gaseous coolant through heat-exchange pipes or coils inside the **chamber** to prevent explosion or firing from activated carbon during O3 decompn. The app. is safe to operate and reduces **lining** cost.

- IC ICM B01D053-66
ICS B01D053-34
- CC 59-4 (Air Pollution and Industrial Hygiene)
Section cross-reference(s): 61, 76
- ST decompn residual ozone **temp control** cooling system
- IT Decomposition catalysts
Waste gases
(app. for decompn. of residual ozone from water **treatment** or **semiconductor** device cleaning)
- IT **Control** apparatus
(**temp.**; in catalytic decompn. of residual ozone from water **treatment** or **semiconductor** device cleaning)
- IT 1313-13-9, Manganese dioxide, uses 1317-38-0, Copper oxide (CuO), uses
(app. for decompn. of residual ozone from water **treatment** or **semiconductor** device cleaning)
- IT 10028-15-6, Ozone, processes
(decompn. of residual; app. for decompn. of residual ozone from water **treatment** or **semiconductor** device cleaning)

L174 ANSWER 7 OF 19 HCA COPYRIGHT 2002 ACS

131:265058 Deposition resistant **lining** for CVD

chamber. Bang, Won B.; Yieh, Ellie; Pham, Thanh (Applied Materials, Inc., USA). PCT Int. Appl. WO 9949102 A1 19990930, 30 pp. DESIGNATED STATES: W: JP, KR; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2. APPLICATION: WO 1999-US6485 19990324. PRIORITY: US 1998-47284 19980324.

- AB A deposition resistant **lining** assembly is provided for a CVD **chamber**, the deposition resistant **lining** assembly including a **1st** ceramic **liner** for mounting adjacent a substrate holder within the CVD **chamber** to protect a portion of an interior wall of the CVD **chamber** from deposition of material on the portion of said interior wall of the CVD **chamber**. The deposition resistant **lining** assembly also includes a **2nd** ceramic **liner** for mounting in a pumping channel formed in a peripheral region of the CVD **chamber** to protect a portion of said pumping channel from deposition of the material on the portion of the pumping channel. The **1st** ceramic **liner** and the **2nd** ceramic **liner** are more resistant to deposition of the material than Al and easier and faster to clean of the material deposited thereon than Al. The ceramic **liners**

include Al nitride and Al oxide.

IC ICM C23C016-44

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76

ST aluminum nitride oxide ceramic **liner CVD chamber**; deposition resistant **liner CVD chamber**

IT Vapor deposition apparatus
(ceramic deposition resistant **liner for CVD chamber**)

IT Semiconductor materials
(ceramic deposition resistant **liner for CVD chamber for processing of wafers or substrates of**)

IT 1344-28-1, Aluminum oxide, uses 24304-00-5, Aluminum nitride
(ceramic deposition resistant **liner for CVD chamber**)

L174 ANSWER 8 OF 19 HCA COPYRIGHT 2002 ACS

130:298816 Semiconductor manufacturing system with getter safety device.
Lorimer, D'Arcy H.; Applegarth, Charles H. (Saes Pure Gas, Inc., USA). PCT Int. Appl. WO 9919048 A1 19990422, 49 pp. DESIGNATED STATES: W: CN, JP, KR, RU, SG; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2. APPLICATION: WO 1998-US21030 19981002. PRIORITY: US 1997-950929 19971015.

AB A semiconductor manufg. system includes a getter-based gas purifier coupled in flow communication with a gas distribution network for a semiconductor fabrication facility. The gas distribution network supplies purified gas to at least one **wafer processing chamber** in the semiconductor fabrication facility. The gas purifier includes a getter column having a metallic **vessel** with an **inlet**, an **outlet**, and a containment wall extending between the **inlet** and the **outlet**. Getter material which purifies gas flowing therethrough by sorbing impurities therefrom is disposed in the **vessel**. A 1st temp. sensor is disposed in a top portion of the getter material. The 1st temp. sensor is located in a melt zone to detect rapidly the onset of an exothermic reaction which indicates the presence of excess impurities in the incoming gas to be purified. A 2nd temp. sensor is disposed in a bottom portion of the getter material. The 2nd temp. sensor is located in a melt zone to detect rapidly the onset of an exothermic reaction which indicates that excess impurities are being backfed into the getter column. First and second high m.p., nonmetallic **liners** are disposed in the **vessel** such that at least some of the top and bottom portions, resp., of the getter material is sepd. from the containment wall of the **vessel**. A getter-based gas purifier, a method of making an integrated circuit device, and a method of protecting a getter column are also described.

IC ICM B01D053-04

ICS C30B025-14; C23C016-44
 CC 48-1 (Unit Operations and Processes)
 Section cross-reference(s): 57, 76
 IT **Ceramics**
 (**liner**; semiconductor manufg. system with getter safety device)
 IT Noble gases, **processes**
 (**semiconductor** manufg. system with getter safety device)
 IT 7782-44-7, Oxygen, **processes**
 (**impurity**; **semiconductor** manufg. system with getter safety device)
 IT 409-21-2, Silicon carbide, uses 1314-23-4, Zirconia, uses 1344-28-1, Alumina, uses 12033-89-5, Silicon nitride, uses 12600-79-2, Zirconium oxide (ZrO₂) 14808-60-7, Quartz, uses
 (**liner**; semiconductor manufg. system with getter safety device)
 IT 7440-37-1P, Argon, **processes** 7440-59-7P, Helium, **processes**
 (**purifn.**; **semiconductor** manufg. system with getter safety device)

L174 ANSWER 9 OF 19 HCA COPYRIGHT 2002 ACS

130:9675 Vertical furnace for the **treatment** of **semiconductor** substrates. Buijze, Jacobus Pieter; Stoutjesdijk, Jeroen Jan; De Ridder, Christianus Gerardus Maria; Stohr, Hubertus Johannes Julius (Asm International N.V., Neth.). PCT Int. Appl. WO 9850606 A1 19981112, 15 pp. DESIGNATED STATES: W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG. (English). CODEN: PIXXD2. APPLICATION: WO 1998-NL246 19980505. PRIORITY: NL 1997-1005963 19970502.

AB The treatment **chamber** in the furnace is delimited by a **liner** of refractory material. To increase the life thereof and in particular to restrict the sensitivity to deposits deposited by the process gas fed through the furnace, it is proposed to make the **liner** of a Si carbide material. To seal the furnace **chamber**, a 2nd **liner** of quartz material is placed around a **liner** of this type and the gap between the **two liners** is flushed.

IC ICM C30B025-08
 ICS C30B031-10; C23C016-44
 CC 76-3 (Electric Phenomena)
 ST refractory **lined** furnace **treatment** **semiconductor** substrate
 IT Furnaces
 Semiconductor device fabrication

- (refractory-lined furnace for treatment of semiconductor substrates)
- IT Coating materials
(refractory; refractory-lined furnace for treatment of semiconductor substrates)
- IT 409-21-2, Silicon carbide, uses 7631-86-9, Silica, uses 107992-37-0, Silicon carbide (SiO-1CO-1)
(refractory-lined furnace for treatment of semiconductor substrates)
- L174 ANSWER 10 OF 19 HCA COPYRIGHT 2002 ACS
129:268944 Short-coupled-path extender for plasma source. Boitnott, Charles A. (Gasonics International, USA). U.S. US 5814154 A 19980929, 5 pp. (English). CODEN: USXXAM. APPLICATION: US 1997-788602 19970123.
- AB A short-coupled-path extender comprises a 2-in.-thick housing that inserts as a spacer between a plasma source and a vacuum chamber in various kinds of semiconductor processing equipment. The spacer housing is generally constructed of Al and is thermally well connected to the vacuum chamber and its liq. cooling system to dispose of the heat it collects from the plasma source flow. The plasma source bolts up to a central inlet port on the spacer housing that leads to a 1st quartz-lined antechamber. The plasma source flow encounters a traverse metal wall at the back of the 1st antechamber and is forced to flow radially outward to a system of small outer ports that connect to a 2nd quartz-lined antechamber. The plasma source flow then collects back together and exits the 2nd antechamber through a central outlet port that bolts up to the plasma source seat on the vacuum chamber.
- IC ICM C23C016-00
NCL 118723000R
CC 76-3 (Electric Phenomena)
ST coupled path extender plasma source; semiconductor processing equipment plasma source; aluminum housing spacer plasma source; quartz lined antechamber plasma source
- IT Semiconductor materials
Vacuum chambers
(short-coupled-path extender between plasma source and vacuum chamber in semiconductor processing equipment)
- IT Plasmatrons
(short-coupled-path extender for plasma source in semiconductor processing equipment)
- IT Metals, uses
(short-coupled-path extender for plasma source in semiconductor processing equipment contg.)
- IT 7631-86-9, Silica, uses
(quartz; short-coupled-path extender for plasma source in semiconductor processing equipment having antechamber lined with)

- IT 7429-90-5, Aluminum, uses
(short-coupled-path extender for plasma source in
semiconductor processing equipment having
spacer with housing from)
- L174 ANSWER 11 OF 19 HCA COPYRIGHT 2002 ACS
127:129690 Apparatus for **semiconductor processing**
and method for cleaning it. Jun, Zhao; Tabata, Atsushi; Cho, Tom;
Qiao, Jianmin; Guo, Xin Sheng; Schreiber, Alex (Applied Materials,
Inc., USA). Eur. Pat. Appl. EP 780490 A1 19970625, 14 pp.
DESIGNATED STATES: R: DE, GB. (English). CODEN: EPXXDW.
APPLICATION: EP 1996-309217 19961217. PRIORITY: US 1995-577862
19951222.
- AB The disclosure relates to a method and app. for limiting residue
buildup in an app. for **semiconductor processing**,
esp. by plasma-enhanced CVD, by **lining** with a
ceramic material the exhaust **plenum** and exhaust manifold
of a processing **chamber**. An air gap provided between the
ceramic **liner** and the processing **chamber** walls
increases the dielec. value of the ceramic **liner**, and
further inhibits the buildup of residues. The ceramic **liner**
retains sufficient heat to allow the elimination of heaters
typically used to heat the Al walls during cleaning, if the cleaning
is commenced immediately after a process step so that the ceramic
retains the necessary heat from the previous processing step. The
provision of an air gap aids in this heating, preventing the ceramic
heat from being drawn off by direct contact with the Al walls. In a
preferred embodiment, the ceramic **liners** are attached to
the **chamber** walls with Teflon screws.
- IC ICM C23C016-44
ICS C30B025-14
- CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
- ST **semiconductor processing chamber**
cleaning; plasma enhanced CVD app cleaning
- IT Semiconductor materials
(ceramic **lining** of exhaust manifolds in
semiconductor processing app. to limit residue
buildup)
- IT Engines
(exhaust manifolds; ceramic **lining** of exhaust manifolds
in **semiconductor processing** app. to limit
residue buildup)
- IT Ceramics
(**liners**; in app. for **semiconductor**
processing to limit residue buildup)
- IT Cleaning
(of **semiconductor processing** app.)
- IT Vapor deposition process
(plasma; cleaning of app. for plasma-enhanced CVD on
semiconductor substrates)
- IT Fluoropolymers, uses

- (screws; for fastening ceramic **lining** of exhaust manifolds in **semiconductor processing** app. to limit residue buildup)
- IT 7429-90-5, Aluminum, uses
(ceramic **lining** of exhaust manifolds in **semiconductor processing** app. having aluminum walls to limit residue buildup)
- IT 1344-28-1, Alumina, processes
(ceramic **lining** of exhaust manifolds in **semiconductor processing** app. to limit residue buildup)
- IT 9002-84-0, Teflon
(screws; for fastening ceramic **lining** of exhaust manifolds in **semiconductor processing** app. to limit residue buildup)

L174 ANSWER 12 OF 19 HCA COPYRIGHT 2002 ACS

127:87361 Method and apparatus for constant composition delivery of hydride gases for **semiconductor processing**.

Ayers, William M. (Electron Transfer Technologies, Inc., USA; Ayers, William M.). PCT Int. Appl. WO 9720965 A1 19970612, 34 pp.

DESIGNATED STATES: W: CN, JP, US; RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2.

APPLICATION: WO 1996-US18836 19961206. PRIORITY: US 1995-8245 19951206.

- AB The present invention provides an electrochem. system and process for the prodn. of very high purity hydride gases and the feed product streams including these hydride gases at const. compn. over extended periods of time. The processes and apparatuses of the invention can employ a **lined** pressure **vessel** within which resides an electrochem. cell including cathode and anode material. The hydride gas produced within the **vessel** exits through a **port** to a manifold which contains an automatic valve to allow exit of the hydride gas. The hydride gas passes through one or more filters. The gas finally exits the manifold through the pressure regulator to the point where it was used in semiconductor fabrication. A source of gas for mixing with the hydride gas is also included.

IC ICM C25B001-00

ICS C25B001-02; C25B009-00; C25D017-00

CC 72-2 (Electrochemistry)

Section cross-reference(s): 49, 76

ST hydride gas electroprodn delivery **semiconductor processing**; phosphine gas electroprodn delivery **semiconductor processing**; arsine gas electroprodn delivery **semiconductor processing**; stibine gas electroprodn delivery **semiconductor processing**; germane gas electroprodn delivery **semiconductor processing**

IT Reduction, electrochemical
(in hydride gas generation for **semiconductor processing**)

- IT Semiconductor materials
(method and app. for const. compn. electroprod. and delivery of
hydride gases for **semiconductor processing**)
- IT Hydrides
(method and app. for const. compn. electroprod. and delivery of
hydride gases for **semiconductor processing**)
- IT 1307-86-4, Cobalt hydroxide $\text{Co}(\text{OH})_3$ 1313-13-9, Manganese oxide
 MnO_2 , uses 1317-61-9, Iron oxide Fe_3O_4 , uses 7439-98-7,
Molybdenum, uses 7440-47-3, Chromium, uses 7440-62-2, Vanadium,
uses 12054-48-7, Nickel hydroxide 18624-44-7, Iron hydroxide
 $\text{Fe}(\text{OH})_2$ 20033-08-3, Manganese oxide MnO_3 20667-12-3, Silver
oxide Ag_2O 21041-93-0, Cobalt hydroxide $\text{Co}(\text{OH})_2$ 155645-82-2,
Silver oxide Ag_2O_2
(anode in electroprod. of hydride gas for **semiconductor
processing**)
- IT 7440-66-6, Zinc, uses 7782-49-2, Selenium, uses
(cathode in electroprod. of hydride gas for
semiconductor processing)
- IT 7440-36-0, Antimony, uses 7440-38-2, Arsenic, uses 7440-56-4,
Germanium, uses 7723-14-0, Phosphorus, uses
(cathode in electroprod. of hydride gas for
semiconductor processing)
- IT 7439-92-1, Lead, uses 7440-43-9, Cadmium, uses
(electrode in electroprod. of hydride gas for
semiconductor processing)
- IT 37382-15-3P, Aluminum gallium arsenide ((Al,Ga)As)
(method and app. for const. compn. electroprod. and delivery of
hydride gases for **semiconductor processing**)
- IT 7782-65-2P, Germane 7783-07-5P, Hydrogen selenide 7784-42-1P,
Arsine 7803-51-2P, Phosphine 7803-52-3P, Stibine
(method and app. for const. compn. electroprod. and delivery of
hydride gases for **semiconductor processing**)
- IT 1310-58-3, Potassium hydroxide, uses 1310-65-2, Lithium hydroxide
1310-73-2, Sodium hydroxide, uses
(method and app. for const. compn. electroprod. and delivery of
hydride gases for **semiconductor processing**
using aq. electrolyte of)

L174 ANSWER 13 OF 19 HCA COPYRIGHT 2002 ACS

125:65398 Synthesis of carbon clusters and thin films by low temperature
plasma **chemical vapor deposition** under
atmospheric pressure. Koinuma, Hideomi; Horiuchi, Takao; Inomata,
Kiyoto; Ha, Hyun-Kwon; Nakajima, Kenji; Chaudhary, Kalik A. (Res.
Lab. Eng. Materials, Tokyo Inst. Technol., Yokohama, 226, Japan).
Pure and Applied Chemistry, 68(5), 1151-1154 (English) 1996. CODEN:
PACHAS. ISSN: 0033-4545. Publisher: Blackwell.

AB Torch-type plasma generator to make low temp. material processing
possible in open air conditions was developed. The cylindrical
plasma **CVD** app. is composed of a metal needle acting as
the cathode at the center and a grounded cylindrical anode. The
inner surface of anode was **lined** by a thin insulator
nozzle. A low temp. homogeneous plasma was generated by

applying rf voltage to the needle cathode under a const. flow of atm. pressure He or AR. The plasma generated in the insulator **nozzle** was released to open air. This cold plasma torch has been verified to be applicable for various plasma processings. Fullerene was found to be formed by the analyses with HPLC to TOF-MS in the soot produced by introducing a vaporized arom. hydrocarbon into the after-glow region of the plasma with Te and Tg at about 1.9 eV and 400.degree.C, resp. Different from the conventionally employed arc-plasma, which decomp. graphite into fullerenes at much higher temps., this is a polycondensation reaction that wraps up small mols. into a large mol. We examd. the possible of using this plasma for encapsulating or incorporating hetero-atom(s) in the fullerene. The plasma was successfully employed for the deposition of such inorg. thin films as glassy carbon, SiO₂, and TiO₂ in open air environment.

- CC 57-8 (Ceramics)
- ST fullerene synthesis CVD plasma reactor; titania film CVD plasma reactor; silica film CVD plasma reactor
- IT Films
(synthesis of carbon clusters and thin films by low temp. plasma chem. vapor deposition under atm. pressure)
- IT Fullerenes
(synthesis of carbon clusters and thin films by low temp. plasma chem. vapor deposition under atm. pressure)
- IT Reactors
Vapor deposition processes
(plasma, synthesis of carbon clusters and thin films by low temp. plasma chem. vapor deposition under atm. pressure)
- IT 7631-86-9P, Silica, preparation 13463-67-7P, Titania, preparation
(synthesis of carbon clusters and thin films by low temp. plasma chem. vapor deposition under atm. pressure)

L174 ANSWER 14 OF 19 HCA COPYRIGHT 2002 ACS

124:43394 Microwave plasma apparatus. Takeshita, Kyoko; Iio, Koichi (Sumitomo Metal Ind, Japan). Jpn. Kokai Tokkyo Koho JP 07272897 A2 19951020 Heisei, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1994-62308 19940331.

AB A microwave plasma app. for etching, ashing and depositing in **semiconductor processing**, wherein the microwave inlet plate consists of a metal plate, and a plurality of dielec. inserts **lining the holes** in the plate.

IC ICM H05H001-46

ICS C23F004-00; H01L021-205; H01L021-3065

CC 76-3 (Electric Phenomena)

ST microwave plasma app **semiconductor processing**

IT **Reactors**

(plasma, microwave; microwave plasma app.)

L174 ANSWER 15 OF 19 HCA COPYRIGHT 2002 ACS

120:205215 Preventing the formation of low-temperature ammonia salts in **CVD** of titanium nitride. Eichman, Eric C.; Sommer, Bruce A.; Churley, Michael J.; Ramsey, W. Chuck (Materials Research Corp., USA). U.S. US 5271963 A 19931221, 6 pp. (English). CODEN: USXXAM. APPLICATION: US 1992-976516 19921116.

AB A cold-wall **CVD reactor**, particularly one for use in depositing TiN in a $\text{TiCl}_4 + \text{NH}_3$ reaction, is provided with a metallic **liner** which is partially thermally insulated from the **reactor** wall and serves as 1 plasma electrode to form a weak secondary plasma when energized along with a 2nd electrode near the vacuum exhaust **port** of the **reactor**. The plasma, in cooperation with radiant lamps provided to heat a wafer substrate onto which the primary **CVD** film is to be applied, heats the **liner** and a portion of the space adjacent the **reactor** walls and susceptor surfaces downstream of the reaction vol. to cause the formation of deposits to be of the nature that can be removed by plasma cleaning without opening the **reactor** vol. Deposits such as TiNxCly and TiN form at .apprx.200-650.degree., preferably 300-450.degree., rather than adduct NH_3 salts of TiCl_4 , which would tend to form at .ltoreq.200.degree..

IC ICM C23C016-00

ICS C23C016-34; C23C016-50

NCL 427248100

CC 75-1 (Crystallography and Liquid Crystals)

Section cross-reference(s): 76

ST ammonia salt formation prevention **CVD**; titanium nitride **CVD**

IT 25583-20-4, Titanium nitride (TiN)

(**CVD** of, prevention of ammonia salt formation in)

L174 ANSWER 16 OF 19 HCA COPYRIGHT 2002 ACS

110:49040 Vertical **chemical vapor deposition**

apparatus. Yamaguchi, Akio (Fujitsu Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 63204717 A2 19880824 Showa, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1987-38508 19870220.

AB The title app. is characterized by upward ejection of the source gas from a **nozzle** located above the substrate, reflection of the gas flow, and changes of reflection angles for momentary interruption of supply of the gas onto the substrate surface. A back-current head was attached to the **nozzle** and an umbrella-shaped gas flow reflector was placed in the upper portion of the reaction **chamber**. An InP layer was grown, the reflector was withdrawn upward, and the gas flow was directed to the outside of the **liner** tube; simultaneously, the supply of PH_3 was switched to AsH_3 , the reflector was lowered to the normal position, and a (Ga,In)As layer was formed. The interface between the layers was abrupt, with a 10-.ANG.-wide transition zone.

IC ICM H01L021-205

CC 75-2 (Crystallography and Liquid Crystals)

ST gas supply abrupt interruption deposition app; reflection gas flow deposition app; indium phosphide VPE; gallium indium arsenide VPE; vertical **chem vapor deposition** app

IT Films
(**chem. vapor deposition** app. for,
with abrupt interruption of gas supply by gas flow reflection)

L174 ANSWER 17 OF 19 HCA COPYRIGHT 2002 ACS

78:105083 Examination of irradiated uranium nitride fuel clad with tungsten-rhenium or T-111 alloy. Cuneo, D. R.; Long, E. L., Jr.; Jostsons, A.; Washburn, T. N. (Oak Ridge Natl. Lab., Oak Ridge, TN, USA). Report, ORNL-TM-3895, 46 pp. Avail. Dep. NTIS From: Nucl. Sci. Abstr. 1973, 27(1), 614 (English) 1972.

AB Three fuel pins contg. UN pellets were irradiated in the thermal n flux of the ORR for 5800 hr to a peak burnup of 1.75 at.%. The pin with 2-25% Re cladding performed satisfactorily with the cladding outer surface at 1300.degree.. The 2 pins with T-111 (Ta-8% W-2% Hf) cladding, which had an inner **liner** of **chem. vapor deposited** W, operated with the cladding outer surface at 1400.degree.. The T-111 on one of the pins failed during the test by intergranular fracture. The grain size in the failed region was 6 times that in the gas **plenum** region, indicating that failure was caused by a localized hot spot. However, numerous cracks and cavities were found in other regions of the T-111 cladding of both the failed and unfailed pins; the cladding on both of these pins would have untimately failed without the hot spot. Hf-rich areas, with concns. 30-40 times that in the homogeneous alloy, were detected by electron microprobe examn. at the cracks and cavities in both the T-111 and the W **liner**. The mechanism of the test-induced concn. of Hf was not detd. The UN fuel performed satisfactorily in all 3 pins. The fission-gas release wqas only 0.1% at 1380.degree. (top pin) and 7.1% at 1500.degree. (bottom pin). Swelling of the fuel was adequately restrained by the cladding and was limited to closing of the as-fabricated 0.005-in. gap between the fuel and cladding. No gross chem. reaction occurred between the fuel and cladding. Although they interacted to a depth of .apprx.20 .mu.m, electron microprobe anal. of the cladding revealed no U penetration beyond that depth. N released from the UN may have interacted with the T-111 and led to the degradation of its mech. properties.

CC 76-6 (Nuclear Technology)

IT Nuclear **reactor** fuels and fuel elements
(uranium nitride, clad with tantalum and tungsten alloys)

IT 11125-19-2 37315-73-4
(claddings, on uranium nitride nuclear-**reactor** fuel)

IT 25658-43-9
(nuclear **reactor** fuel, clad with tantalum and tungsten alloys)

L174 ANSWER 18 OF 19 HCA COPYRIGHT 2002 ACS

75:26988 Silicon nitride **linings** on quartz tubes for semiconductor diffusion or oxidation. Pammer, Erich; Folkmann,

Eduard (Siemens A.-G.). Ger. Offen. DE 1957952 19710527, 9 pp.
(German). CODEN: GWXXBX. APPLICATION: DE 19691118.

AB Si nitride coatings (optionally contg. Si carbide) on quartz tubes for semiconductor diffusion or oxidn. processes are manufd. by pyrolysis of 1:10 $\text{SiH}_4\text{-NH}_3$ mixt. in N optionally contg. CH_4 at 800-900.degree. and annealing at 1200.degree.. The app. consists of a ring burner and an annealing **chamber** in series through which the quartz tube is drawn. The quartz tube contains a feed pipe and distributing head with radial **nozzles** through which the gases are directed to the pyrolysis zone.

IC B01J

CC 71 (Electric Phenomena)

IT Diffusion

(in elec.-**semiconductor processing**,
lining of quartz tubes with silicon nitride for)

IT **Lining** process

(of quartz tubes with silicon nitride for **semiconductor processing**)

IT Semiconductors, electric

(quartz tubes for processing of, **lining** with silicon nitride of)

IT 14808-60-7, uses and miscellaneous

(**lining** of tubes from, with silicon nitride)

IT 12033-89-5

(**lining** with, of quartz tubes for **semiconductor processing**)

L174 ANSWER 19 OF 19 HCA COPYRIGHT 2002 ACS

72:94576 **Semiconductor** material **treatment** furnace.

Kagdis, William A.; Tanski, John J. (United States Dept. of the Navy). U.S. US 3493220 19700203, 5 pp. (English). CODEN: USXXAM.
APPLICATION: US 19680307.

AB A treatment furnace is described, wherein a gas is admitted into one end of a vertical **chamber** and is extd. from the other end; the gas comes in contact with and treats a no. of semiconductor wafers suspended in the **chamber**. The furnace consists of a vertically oriented heating **chamber** around which is a heat source. The **chamber** is provided with a gas **inlet** at the lower end and a gas **outlet** at its upper end. Wafers are placed in a basket which is suspended along the **chamber** axis by a rod and wire. The remote control system assocd. with the wire can raise or lower the basket and also impart rotational motion. A screen is placed across the **chamber** to insure uniform gas diffusion. The gas as it passes through the screen experiences turbulence in the treating region. The action of the rotating wafers and turbulence assures that every part of the wafer is diffused alike. A **liner**, supported in the **chamber**, is adaptable for easy replacement after it becomes impregnated with diffusing gas. Thus, only the **liner** needs periodic replacement. The furnace is provided with means for protecting the wafers against contact with the diffusion gas during the thermal lag or recovery time of the

furnace just after the wafers are inserted into the **chamb r**
 . The furnace is readily adaptable to automation, so that a loaded basket can travel from a loading platform to the furnace, be treated, and then return to the loading platform automatically. The furnace is also provided with an exhaust hood which removes the treating gas after it has been used.

IC F27B; C23C
 NCL 263041000
 CC 71 (Electric Phenomena)
 ST **semiconductor wafers** diffusion treatment
 ; diffusion treatment **semiconductor**
wafers; wafers semiconductor diffusion
 treatment
 IT Furnaces
 (for gas treatment of **semiconductors** in
 diffusion doping)

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L175 ANSWER 1 OF 6 HCA COPYRIGHT 2002 ACS

136:46010 **Temperature controlled** gas feedthrough.

Sajoto, Talex; Dornfest, Charles; Selyutin, Leonid; Zhao, Jun; Ku, Vincent; Jin, Xiao-Liang (Applied Materials, Inc., USA). PCT Int. Appl. WO 2001098556 A2 20011227, 64 pp. DESIGNATED STATES: W: JP, KR; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2001-US19118 20010615. PRIORITY: US 2000-595767 20000616.

AB The invention relates to an app. and process for the vaporization of liq. precursors and deposition of a film on a suitable substrate. In one aspect, an app. and process for the control of a gas flowed through a gas feedthrough in a substrate processing **chamber** and system is provided. In another aspect, a deposition **chamber** is provided for depositing BST and other materials which require vaporization, esp. low volatility precursors which are transported as a liq. to a vaporizer to be converted to vapor phase and which must be transported at elevated temps. to prevent unwanted condensation on **chamber** components. The **chamber** comprises heated **temp. controlled** internal **liners**, such as a heated gas feedthrough.

IC ICM C23C016-44
 CC 75-1 (Crystallography and Liquid Crystals)
 Section cross-reference(s): 76
 ST **temp controlled** gas feedthrough CVD
 app

IT Vapor deposition apparatus
 (**temp. controlled** gas feedthrough for
 vaporization of liq. precursors and deposition of film on
 suitable substrate)

IT 7440-06-4, Platinum, processes 7440-21-3, Silicon, processes
 7631-86-9, Silicon oxide (SiO₂), processes
 (**temp. controlled** gas feedthrough for

- deposition of film on Pt/SiO₂/Si)
- IT 37305-87-6, Barium strontium titanate
(**temp. controlled** gas feedthrough for
vaporization of liq. precursors and deposition of film on
suitable substrate)
- IT 144665-26-9 158595-98-3 177645-16-8
(**temp. controlled** gas feedthrough for
vaporization of liq. precursors of)
- L175 ANSWER 2 OF 6 HCA COPYRIGHT 2002 ACS
136:8253 **Semiconductor process chamber**
having improved **temperature control**.
Shamouilian, Shamouil; Kumar, Ananda H.; Narendrnath, Kadthala R.;
Askarinam, Eric; Weldon, Edwin C.; Rice, Michael; Collins, Kenneth
S. (USA). U.S. Pat. Appl. Publ. US 20010042594 A1 20011122, 13 pp.,
Cont.-in-part of U.S. 6,074,512. (English). CODEN: USXXCO.
APPLICATION: US 1998-82430 19980520. PRIORITY: US 1996-648254
19960513; US 1996-733555 19961021; US 1997-893393 19970715.
- AB A **temp. control** system is used to
control the **temp.** of a process **chamber**
during **processing** of a **semiconductor** substrate.
The **temp. control** system comprises a heat
exchanger plate for removing heat from the **chamber**, and a
heat transfer member for conducting heat to the heat exchanger
plate. The heat transfer member comprises a lower heat conduction
surface bonded to an external surface of the **chamber**, and
an upper heat transmitting surface thermally coupled to the heat
exchanger plate. Preferably, the **temp. control**
assembly comprises a heater for heating the **chamber**, and a
computer control system for regulating the heat removed by the heat
exchanger plate as well as the heat supplied by the heater, to
maintain the **chamber** at substantially uniform temps.
- IC ICM C23F001-02
ICS C23C014-00
- NCL 156345000
- CC 47-10 (Apparatus and Plant Equipment)
Section cross-reference(s): 76
- ST **semiconductor process chamber**
temp control
- IT Electric coils
(antenna; **semiconductor process**
chamber having improved **temp. control**
)
- IT Hydrocarbons, uses
(fluoro, heat exchange fluid; **semiconductor**
process chamber having improved **temp.**
control)
- IT Plasma
(generated by electrode; **semiconductor process**
chamber having improved **temp. control**
)
- IT Adhesives

(heat-conductive; semiconductor process chamber having improved temp. control)
)

IT Antennas
(inductor; semiconductor process chamber having improved temp. control)
)

IT Pyrometers
(optical, temp. sensor; semiconductor process chamber having improved temp. control)
)

IT Heat exchangers
(perfluorinated liq., Galden, Fluorinert; semiconductor process chamber having improved temp. control)
)

IT Polyesters, uses
(release sheet; semiconductor process chamber having improved temp. control)
)

IT Degreasing
Heaters
(semiconductor process chamber having improved temp. control)
)

IT Computer program
(temp. control; semiconductor process chamber having improved temp. control)
)

IT Thermocouples
(temp. sensor; semiconductor process chamber having improved temp. control)
)

IT Polyimides, uses
(thermally conductive adhesives; semiconductor process chamber having improved temp. control)
)

IT Epoxy resins, uses
(thermally conductive adhesives; semiconductor process chamber having improved temp. control)
)

IT Semiconductor materials
(wafer; semiconductor process chamber having improved temp. control)
)

IT 1303-00-0, Gallium arsenide, uses 7440-56-4, Germanium, uses 22398-80-7, Indium phosphide, uses 29870-72-2, Mercury cadmium telluride
(RF conducting ceiling; semiconductor process chamber having improved temp. control)
)

IT 1344-28-1, Aluminum oxide, uses 7429-90-5, Aluminum, uses 7440-21-3, Silicon, uses 12069-32-8, Boron carbide 12597-68-1, Stainless steel, uses 12606-02-9, INCONEL 14808-60-7, Quartz,

uses
(chamber made of; semiconductor
process chamber having improved temp.
control)

IT 88385-83-5, Oakite
(degreasing; semiconductor process
chamber having improved temp. control
)

IT 10043-11-5, Boron nitride, uses
(dowel pin; semiconductor process
chamber having improved temp. control
)

IT 7439-98-7, Molybdenum, uses 7440-25-7, Tantalum, uses 7440-33-7,
Tungsten, uses
(electrode embedded in dielec. materials; semiconductor
process chamber having improved temp.
control)

IT 7440-50-8, Copper, uses
(heat exchanger made of; semiconductor process
chamber having improved temp. control
)

IT 7440-59-7, Helium, uses
(heat transfer gas; semiconductor process
chamber having improved temp. control
)

IT 7732-18-5, Water, uses
(high resistivity, heat exchange fluid; semiconductor
process chamber having improved temp.
control)

IT 24304-00-5, Aluminum nitride
(in for comprising electrode; semiconductor
process chamber having improved temp.
control)

IT 409-21-2, Silicon carbide, uses 12033-89-5, Silicon nitride, uses
(in for comprising electrode; semiconductor
process chamber having improved temp.
control)

IT 1314-23-4, Zirconium oxide, uses 7631-86-9, Silica, uses
(lining materials for silicon ceiling;
semiconductor process chamber having
improved temp. control)

IT 25038-59-9, Mylar, uses
(release sheet; semiconductor process
chamber having improved temp. control
)

IT 7647-01-0, Hydrochloric acid, uses 7664-39-3, Hydrofluoric acid,
uses 7664-93-9, Sulfuric acid, uses 7697-37-2, Nitric acid, uses
7722-84-1, Hydrogen peroxide, uses
(silicon ceiling cleaning soln.; semiconductor
process chamber having improved temp.
control)

L175 ANSWER 3 OF 6 HCA COPYRIGHT 2002 ACS

134:334534 Modified thermocouple mounting bushing and system including the same. Ramos, Jesse C.; Foster, Blake A.; Nelson, Allan T. (Advanced Micro Devices, Inc., USA). U.S. US 6224678 B1 20010501, 9 pp. (English). CODEN: USXXAM. APPLICATION: US 1998-132831 19980812.

AB An **LPCVD** system is provided in which a thermocouple mounting system is configured to inhibit motion of a thermocouple with respect to an **LPCVD reactor**. The thermocouple mounting system includes an improved thermocouple mounting bushing that forms a fixable engagement with a thermocouple mounting hub. The thermocouple mounting bushing compresses a clip ring against both the thermocouple and the thermocouple mounting hub during use to inhibit motion of the thermocouple. The improved thermocouple mounting system inhibits contact between the thermocouple and a quartz **liner** within the **reactor** during use, thus minimizing formation of contaminating particles. The thermocouple mounting system further maintains the thermocouple in proper alignment according to design criteria such that accurate temp. readings are supplied to a **temp. controller** during use. In addn., the improved thermocouple mounting system prevents the thermocouple from being pulled into the **reactor** during use in the event an O-ring, also part of the thermocouple mounting system, is weakened or fails.

IC ICM C23C016-00

NCL 118715000

CC 75-1 (Crystallography and Liquid Crystals)

Section cross-reference(s): 76

ST thermocouple mounting bushing **LPCVD**

IT Integrated circuits

Thermocouples

(**CVD** system for integrated circuit fabrication employing modified thermocouple mounting bushing)

IT Vapor deposition apparatus

(low-pressure; **CVD** system for integrated circuit fabrication employing modified thermocouple mounting bushing)

L175 ANSWER 4 OF 6 HCA COPYRIGHT 2002 ACS

133:275226 Low contamination high density plasma etch **chambers** and methods for making the same. Wicker, Thomas E.; Maraschin, Robert A.; Kennedy, William S. (LAM Research Corporation, USA). U.S. US 6129808 A 20001010, 19 pp., Cont.-in-part of U.S. Ser. No. 50,902, abandoned. (English). CODEN: USXXAM. APPLICATION: US 1998-161074 19980925. PRIORITY: US 1998-50902 19980331.

AB A high d. plasma processing **chamber** including an electrostatic chuck for holding a wafer, and consumable parts that are highly etch resistant, less susceptible to generating contamination and **temp. controllable** is disclosed. The consumable parts include a **chamber liner** having a lower support section and a wall that is configured to surround the electrostatic chuck. The consumable parts also include a **liner** support structure having a

lower extension, a flexible wall, and an upper extension. The flexible wall is configured to surround an external surface of the wall of the **chamber liner**, and the **liner support flexible wall** is spaced apart from the wall of the **chamber liner**. The lower extension of the **liner support** is however, configured to be in direct thermal contact with the lower support section of the **chamber liner**. Addnl., a baffle ring is part of the consumable parts, and is configured to be assembled with and in thermal contact with the **chamber liner** and the **liner support**. A heater is capable of being thermally connected to the **liner support** for thermally conducting a temp. from the **liner support** to the **chamber liner** and the baffle ring. In a most preferred embodiment, the **chamber liner** and the baffle ring are made from materials that are innocuous to materials on the **wafer** being **etched**. In this manner, once these materials are exposed to the energy of the high d. plasma sputtering, volatile products will be produced that are substantially similar to volatile etch products produced during the etching of surface layers of the wafer. These volatile products can then be removed from the **chamber**.

IC ICM H05H001-00
 NCL 156345000
 CC 76-3 (Electric Phenomena)
 ST low contamination high density plasma etching **chamber**
 IT Etching
 Etching apparatus
 Plasma
 Semiconductor device fabrication
 Sputtering
 Thermal conductivity
 (low contamination high d. plasma etch **chambers** and
 methods for making the same)

L175 ANSWER 5 OF 6 HCA COPYRIGHT 2002 ACS

132:245066 Low-contamination high-density plasma etching **chamber**
 and **processing** of **semiconductor** substrates using
 it. Wicker, Thomas E.; Maraschin, Robert A.; Kennedy, William S.
 (Lam Research Corporation, USA). PCT Int. Appl. WO 2000019481 A2
 20000406, 39 pp. DESIGNATED STATES: W: AE, AL, AM, AT, AU, AZ, BA,
 BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB,
 GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
 LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO,
 RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN,
 YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ,
 CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU,
 MC, ML, MR, NE, NL, PT, SE, SN, TD, TG. (English). CODEN: PIXXD2.
 APPLICATION: WO 1999-US20890 19990924. PRIORITY: US 1998-161074
 19980925.

AB A high-d. plasma processing **chamber** including an
 electrostatic chuck for holding a wafer, and consumable parts that

are highly etch resistant, less susceptible to generating contamination, and **temp. controllable** is disclosed. The consumable parts include a **chamber liner** having a lower support section and a wall that is configured to surround the electrostatic chuck. The consumable parts also include a **liner** support structure having a lower extension, a flexible wall, and an upper extension. The flexible wall is configured to surround the wall of the **chamber liner**, and the **liner** support flexible wall is spaced apart from the wall of the **chamber liner**. The lower extension of the **liner** support is configured to be in direct thermal contact with the lower support section of the **chamber liner**. Addnl., a baffle ring is part of the consumable parts, and is configured to be assembled with and in thermal contact with the **chamber liner** and the **liner** support. A heater is capable of being thermally connected to the **liner** support for thermally conducting heat from the **liner** support to the **chamber liner** and the baffle ring. In a most preferred embodiment, the **chamber liner** and the baffle ring are made from materials that are innocuous to materials on the **wafer** being **etched**. In this manner, once these materials are exposed to the energy of the high-d. plasma sputtering, volatile products are produced that are substantially similar to volatile products produced during the etching of surface layers of the **wafer**. These volatile products can then be removed from the **chamber**.

- IC ICM H01J037-00
- CC 76-11 (Electric Phenomena)
- ST plasma **etching chamber semiconductor**
substrate **processing**
- IT Holders
(chucks, electrostatic; low-contamination high-d. plasma etching **chamber** for **processing** of **semiconductor** substrates contg.)
- IT Sputtering
(in low-contamination high-d. plasma etching **chamber** for **processing** of **semiconductor** substrates)
- IT Semiconductor device fabrication
(low-contamination high-d. plasma etching **chamber** for)
- IT Semiconductor materials
(low-contamination high-d. plasma etching **chamber** for **processing** of **semiconductor** substrates)
- IT Baffles
Ceramics
Heaters
(low-contamination high-d. plasma etching **chamber** for **processing** of **semiconductor** substrates contg.)
- IT Etching apparatus
(plasma; low-contamination high-d. plasma etching **chamber** for **processing** of **semiconductor** substrates)
- IT Volatile substances

(removal of; from low-contamination high-d. plasma etching chamber for processing of semiconductor substrates)

IT 409-21-2, Silicon carbide (SiC), uses 10043-11-5, Boron nitride, uses 12033-89-5, Silicon nitride, uses 12069-32-8, Boron carbide (B4C)

(low-contamination high-d. plasma etching chamber for processing of semiconductor substrates contg.)

L175 ANSWER 6 OF 6 HCA COPYRIGHT 2002 ACS

14:11699 Original Reference No. 14:2164e-i,2165a Manufacture of lethal gases in Germany. Carr, Francis H. J. Soc. Chem. Ind., 38, 468R (Unavailable) 1919.

AB For the prepn. of mustard gas, thiodiglycol was made at the Badische works and combined with HCl at the Bayer plant. C₂H₄ was prepd. by the action of Al₂O₃ on EtOH vapor in a Cu tube at 400.degree.; the catalyst remained active for 10 days. The gas was then passed with CO₂ into bleaching powder stirred with H₂O, the mixt. being cooled to 5.degree.; after 3-4 hrs. the CaCO₃ was filtered off in presses, and the CH₂(OH)CH₂Cl soln. concd. to 20%. This product was formerly used in indigo synthesis, and the greatly enlarged production is now available for dye manuf. Conversion of CH₂(OH)CH₂Cl to thiodiglycol was the next step, followed by concn. and sepn. of NaCl, after which the product was sent to the Bayer works in tank wagons, where HCl gas was passed in through glass tubes. Glass hoods and exhaust ducts above and below the reaction vessels, which were 7 ft. in diam. and 6 ft. deep, effectively removed fumes, a fact which, combined with great care in all steps and continual supervision by the works chemists, prevented all but one casualty. After washing and removal of volatile compds. by vacuum distn., the mustard gas was dild. with CCl₄ and sent to the shell-filling plant. For As compds., PhN₂Cl was coupled with NaAsO₂ in the presence of a little Cu, and the phenylarsenic acid reduced with SO₂, after which the phenylarsenous acid was sent to another plant, coupled with PhN₂Cl, and the diphenylarsenic acid reduced as before. Conversion into the chloride by means of HCl took place in a third plant. The yields were 60-70%. The cyanide was easily made from the chloride by means of KCN. Ethyldichloroarsine was prepd. from EtCl and AS₂O₃ at 100.degree., giving ethylarsenious oxide, which was then chlorinated under 12 atm. and treated with H₂SO₄ and Na₂SO₃. Dichloromethyl ether was prepd. from ClSO₃H and paraformaldehyde in H₂SO₄, the HCl being blown out by air. Diphosgene was very troublesome, and there were many casualties from escaping gases. Chlorination of HCO₂Me took place in the-lined vessels, the temp. being controlled carefully, and the reaction being aided by the light from 4000-c. p. Osram lamps. Other compds. made were brominated acetone, Me₂SO₄, and phenylcarbylamine chloride. In the prepn. of activated charcoal, the wood chips were first treated with HCl and a little ZnCl₂, then charred and washed, the small % of Zn producing a very absorptive charcoal.

CC 10 (Organic Chemistry)

=> file wpix

FILE 'WPIX' ENTERED AT 17:29:46 ON 04 OCT 2002
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=> d l165 1-42 max

L165 ANSWER 1 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-589328 [63] WPIX

DNN N2002-467587.

TI Thermally controlled processing **chamber liner**
used in **semiconductor wafer processing**
system, has passage provided to base and inner wall of
chamber for fluid flow from fluid source.

DC U11 V05

IN CARDUCCI, J D; LEE, E; LUSCHER, P; NOORBAKSH, H; SALIMIAN, S; SHAN,
H; VAIDYA, K; WELCH, M D

PA (MATE-N) APPLIED MATERIALS INC

CYC 1

PI US 2002069970 A1 20020613 (200263)* 17p C23F001-02

ADT US 2002069970 A1 Div ex US 2000-519719 20000307, US 2002-55310
20020122

PRAI US 2000-519719 20000307; US 2002-55310 20020122

IC ICM C23F001-02

ICS C23C016-00

AB US2002069970 A UPAB: 20021001

NOVELTY - An etch **chamber** (100) has a **liner**
(104) provided with a base. An inner wall is connected to the base.
A passage having **inlet** and **outlet**, is provided
to the base and the inner wall for fluid flow from a
temperature controlled fluid source (121).

USE - For **lining** a processing **chamber** used
in **semiconductor wafer processing**
system.

ADVANTAGE - Reduces stress formation on the films deposited on
the **chamber liner** which increases the service
life of the **liner** and minimizes film fracture and the
associated particulate generation by maintaining a predetermined
constant temperature.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional
view of a **semiconductor wafer processing**
system.

Etch **chamber** 100

Liner 104

Fluid source 121

Dwg.1/7

TECH US 2002069970 A1UPTX: 20021001

TECHNOLOGY FOCUS - METALLURGY - The base of the thermally controlled
processing **chamber** is made of a material selected from a
group of aluminum, ceramic and stainless steel.

FS EPI

FA AB; GI

MC EPI: U11-C09C; U11-C09F; V05-F05C; V05-F05E9; V05-F09

L165 ANSWER 2 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-557163 [59] WPIX

DNN N2002-441070 DNC C2002-157946

TI **Chamber liner** for vapor deposition apparatus, includes inner annular portion containing material resistant to process gases, and outer annular portion comprising insulating material.

DC L03 T01 U11 U13 V05

IN FRANKEL, J; SIVARAMAKRISHNAN, V

PA (FRAN-I) FRANKEL J; (SIVA-I) SIVARAMAKRISHNAN V; (MATE-N) APPLIED MATERIALS INC

CYC 1

PI US 2002073922 A1 20020620 (200259)* 80p C23C016-00

US 6444037 B1 20020903 (200260) C23C016-00

ADT US 2002073922 A1 US 1996-746748 19961113; US 6444037 B1 US 1996-746748 19961113

PRAI US 1996-746748 19961113

IC ICM C23C016-00

AB US2002073922 A UPAB: 20020916

NOVELTY - A **chamber liner** comprises an inner annular portion containing material that is resistant to process gases at at least 400 deg. C, and an outer annular portion disposed adjacent the inner portion and comprising an insulating material for decreasing a thermal gradient between the perimeter of the water and enclosure.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for an apparatus for fabricating an integrated circuit device comprising an enclosure housing (200) a processing **chamber** (15) and having gas **inlet** and **outlet**, a pedestal disposed in the processing **chamber** for supporting a wafer, and the inventive **chamber liner** (35).

USE - For a vapor deposition apparatus used to deposit doped dielectric films, e.g. borophosphosilicate glass films, borosilicate glass or phosphosilicate glass films; to form ultra-shallow doped regions used, e.g. as source/drain junctions or as channel stop diffusions in shallow trench isolation; and to deposit undoped dielectric films, e.g. undoped silicate glass films use as shallow trench isolation filling oxides, insulating layers, capping layers, or other layers.

ADVANTAGE - The invention allows multiple process steps to be performed in situ in the same **chamber** to reduce total processing time and to ensure high quality processing for high aspect ratio devices. It increases the control of the process parameters and reduces device damage due to metal contamination or process residue contamination. It provides high temperature deposition, heating and efficient cleaning for forming dielectric films having thickness uniformity, good gap fill capability, high density, low moisture, and other desired characteristics.

DESCRIPTION OF DRAWING(S) - The figure shows a vertical

cross-sectional view of a **chemical vapor deposition** apparatus.

Processing **chamber** 15

Chamber liner 35

Enclosure housing 200

Dwg.1/28

TECH US 2002073922 A1UPTX: 20020916

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The inner and outer portions are separated from each other. The outer portion comprises a material resistant to cracking at above 400degreesC. The inner portion comprises a material resistant to the process gas at at least60degreesC without reacting with the process gases and to deposition by the process gas on the pedestal. It is also resistant to etching by fluorine-containing compounds at at least400degreesC. A cover is included overlying at least the outer portion of the **chamber**. The outer portion defines air gap(s) to increase thermal insulation provided by the outer portion. Preferred Property: The outer portion has a thickness greater than that of inner portion. The inner portion is 0.2-0.3 inch thick. The outer portion is 0.8-1.2 inch thick.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The inner portion comprises a ceramic material or aluminum oxide. The outer portion comprises aluminum or its alloy. The cover comprises a ceramic material. The process gas tetraethylorthosilicate, nitrogen fluoride, nitrogen, ozone, oxygen, triethylphosphate, or triethylborate.

FS CPI EPI

FA AB; GI

MC CPI: L04-D01

EPI: T01-J; U11-C09B; U13-D; V05-F

L165 ANSWER 3 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-509025 [54] WPIX

DNN N2002-402826 DNC C2002-144810

TI **Semiconductor processing** equipment component

coating process e.g. for **chamber** walls, substrate supports, involves depositing carbonitride coating on component to form outer erosion resistant surface.

DC L02 M13 U11

IN CHANG, C C; DAUGHERTY, J E; O'DONNELL, R J

PA (CHAN-I) CHANG C C; (DAUG-I) DAUGHERTY J E; (ODON-I) O'DONNELL R J;
(LAMR-N) LAM RES CORP

CYC 99

PI WO 2002053794 A1 20020711 (200254)* EN 22p C23C014-06

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ
DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP
KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ
NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA
UG US UZ VN YU ZA ZW

US 2002094378 A1 20020718 (200255) C23C016-00
ADT WO 2002053794 A1 WO 2001-US43150 20011121; US 2002094378 A1 US
2000-750251 20001229

PRAI US 2000-750251 20001229

IC ICM C23C014-06; C23C016-00

ICS B01J019-02; C23C016-44; C23C016-46; H01L021-00

AB WO 200253794 A UPAB: 20020823

NOVELTY - Two intermediate coatings are deposited one on top of the other on an aluminum substrate. A carbonitride coating is deposited on the substrate to form an outer erosion resistant surface.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **semiconductor processing** equipment component.

USE - For coating **semiconductor processing** equipment component (claimed) such as vacuum **chambers**, substrate supports, rings, **nozzles**, fasteners, **liners**, plasma screens, baffles, etc.

ADVANTAGE - The erosion resistant surface protects underlying materials from the corrosive effects of plasma **chamber** gases, while resisting erosion of the coating by the plasma **chamber** gases.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of plasma **reactor chamber** having a component coated with corrosion resistant coating.

Vacuum processing **chamber** 10

Window 20, 50

Antenna 40

Gas distribution plate 52

Substrate holder 70

Electrostatic clamp 74

Dwg.1/2

TECH WO 200253794 A1UPTX: 20020823

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The carbonitride coating comprises an element from the group of IIB, IIIB, IVB, VB, VIB or VIIB of the periodic table.

FS CPI EPI

FA AB; GI

MC CPI: L02-H02B2; M13-E02; M13-F02

EPI: U11-C09B; U11-C09C; U11-C09E

L165 ANSWER 4 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-463430 [49] WPIX

DNN N2002-365344 DNC C2002-131802

TI Thermally controlled **reactor** for **semiconductor wafer processing** system, has thermally controlled substrate supported within vacuum **chamber** with gas **inlet** and **outlet** and interior surface having thermally controlled lines.

DC E16 L03 U11

IN BJORKMAN, C; CHANG, M; DOAN, K L; KIM, Y; KOMATSU, T; LIU, J; PU, B Y; SHAN, H; WANG, J; WANG, R; CARDUCCI, J D; LEE, E Y; LUSCHER, P E; NOORBAKHS, H; SALIMIAN, S; WANG, Z; WELCH, M D

PA (MATE-N) APPLIED MATERIALS INC

CYC 22

PI WO 2002037541 A2 20020510 (200249)* EN 91p H01L021-00
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR

US 6403491 B1 20020611 (200249) H01L021-3065

ADT WO 2002037541 A2 WO 2001-US46012 20011101; US 6403491 B1 US
2000-704867 20001101

PRAI US 2000-704972 20001101; US 2000-704867 20001101

IC ICM H01L021-00; H01L021-3065

AB WO 200237541 A UPAB: 20020802

NOVELTY - A thermally controlled **reactor** for plasma etch processing substrates at subatmospheric pressures comprises:

- (a) a vacuum **chamber** having a gas **inlet**, gas **outlet** and interior surface;
- (b) a thermally controlled **liner** having internal fluid passage, arranged adjacent to interior surface; and
- (c) a thermally controlled substrate support disposed within the vacuum **chamber**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of plasma etching features on a dielectric layer on a substrate disposed in a magnetically enhanced thermally controlled plasma etch **chamber**, comprising:

- (i) disposing a substrate in a processing region of a thermally controlled plasma etch **chamber**;
- (ii) **controlling** the **temperature** of a wall disposed adjacent to the processing region to create a low temperature that is conducive to adhesion of polymer by-product on the wall;
- (iii) **controlling** the **temperature** of a substrate support;
- (iv) maintaining a pressure in the processing region;
- (v) flowing a gas composition into the processing region;
- (vi) coupling RF energy into the processing region to form a plasma from the gas composition; and
- (vii) providing a magnetic field in the processing region and transverse to the substrate.

USE - For **semiconductor wafer processing** system and for etching dielectric film.

ADVANTAGE - Provides expanded processing capabilities with improved process parameter control that enables improved etching of dielectric.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of parallel plate **semiconductor wafer processing** systems.

Dwg.1/38

TECH WO 200237541 A2UPTX: 20020802

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Substrate: The thermally controlled substrate support is formed from ceramic material. The substrate support further comprises a support plate having a fluid channel and a thermally conductive layer formed from a pressure sensitive acrylic adhesive which comprises a metal or metal alloy. The metal alloy is titanium diborate.

Preferred Method: The gas composition comprises a fluorocarbon, an oxygen comprising gas and an inert gas, having a total flow of 400-800 sccm. Preferably, the fluorocarbon gas is hexafluoro-1,3-butadiene and the oxygen containing gas is O₂.

ABEX WO 200237541 A2UPTX: 20020802

EXAMPLE - No relevant example given.

KW [1] 281214-0-0-0 CL; 217-0-0-0 CL

FS CPI EPI

FA AB; GI; DCN

MC CPI: E10-H04A3; E31-D02; L04-D04

EPI: U11-C07A1; U11-C09C

DRN 1779-U

CMC UPB 20020802

M3 *01* H6 H601 H607 H609 H683 H684 H689 H7 H724 M280 M314 M321
M332 M344 M363 M391 M416 M782 M904 M905 Q454 R013

DCN: RA1P04-K; RA1P04-M

M3 *02* C108 C550 C810 M411 M782 M904 M905 M910 Q454 R013

DCN: R01779-K; R01779-M

L165 ANSWER 5 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-238364 [29] WPIX

CR 2001-475316 [51]; 2001-637965 [73]

DNN N2002-183631 DNC C2002-071897

TI High pressure oxidation of semiconductor device by annealing in a dinitrogen oxide atmosphere and using a catalyst to prevent it becoming super-critical.

DC L03 U11

IN AL-SHAREEF, H N; CHAPEK, D; DEBOER, S; GEALY, F D; THAKUR, R; GEALY, D

PA (ALSH-I) AL-SHAREEF H N; (CHAP-I) CHAPEK D; (DEBO-I) DEBOER S;
(GEAL-I) GEALY F D; (THAK-I) THAKUR R; (MICR-N) MICRON TECHNOLOGY INC

CYC 1

PI US 2001044219 A1 20011122 (200229)* 7p H01L021-31

US 6423649 B1 20020723 (200254) H01L021-31

ADT US 2001044219 A1 Cont of US 1999-386941 19990831, US 2001-910168
20010720; US 6423649 B1 Cont of US 1999-386941 19990831, US
2001-910168 20010720

FDT US 2001044219 A1 Cont of US 6291364; US 6423649 B1 Cont of US
6291364

PRAI US 1999-386941 19990831; US 2001-910168 20010720

IC ICM H01L021-31

ICS H01L021-469

AB US2001044219 A UPAB: 20020823

NOVELTY - Oxidation of a gate dielectric layer and a cell dielectric layer on a silicon substrate that is heated to at least 600 degreesC uses a gaseous dinitrogen oxide (N₂O) atmosphere at a pressure of ca. 5 atmospheres, part of which is in contact with a catalytic matrix (20).

DETAILED DESCRIPTION - A further 8 INDEPENDENT CLAIMS are included for the process described above including processes where the silicon substrate is heated to 600-800 degreesC and the pressure

of the N2O atmosphere is 5-25 atmospheres.

USE - Oxidation of semiconductor device.

ADVANTAGE - By preventing the N2O from becoming super-critical, the reaction is **controlled** to prevent **temperature** and pressure spikes so ensuring uniform **processing** of **semiconductor wafers**. As temperatures in excess of 800 degreesC are not needed due to the high pressure in the furnace, the wafers are not warped and damaged which can lead to inhibition of the oxide growth layer. The wafers are exposed for a minimal time to the raised temperatures so undesirable dopant diffusion is minimised.

DESCRIPTION OF DRAWING(S) - The diagram illustrates the high pressure furnace used in the process described above.

High pressure furnace 10

Reactor vessel 12

Catalyst matrix **liner** 20

Dwg.3/3

TECH US 2001044219 A1UPTX: 20020508

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The process further oxidises a tantalum oxide layer on the silicon substrate, or forms a barium strontium titanium oxide layer or strontium bismuth titanate oxide layer on part of the substrate.

TECHNOLOGY FOCUS - METALLURGY - Preferred Catalytic Matrix: The matrix is selected from lead, platinum, iridium or palladium, rhodium, nickel or silver.

FS CPI EPI

FA AB; GI

MC CPI: L04-C12A; L04-C16

EPI: U11-C03A

L165 ANSWER 6 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-204132 [26] WPIX

DNN N2002-155181

TI Furnace injector system for thermal **processing** of **semiconductors**.

DC Q77 U11

IN CLEAVER, M P; FUNK, L J; MCHUGH, P R; WILSON, G J

PA (SEMI-N) SEMITool INC

CYC 1

PI US 6191388 B1 20010220 (200226)* 7p F27B005-14

ADT US 6191388 B1 US 1998-195327 19981118

PRAI US 1998-195327 19981118

IC ICM F27B005-14

AB US 6191388 B UPAB: 20020424

NOVELTY - An injector for a vertical furnace with a pedestal, a process **container** enclosing a process **chamber**, and a semiconductor article support on the pedestal, comprises an elongated tube extending from below into the process **chamber**. The tube has a discharge end above the semiconductor support and a circuitous section below it, and a straight section between them.

DETAILED DESCRIPTION - The process **chamber** is

positionable to enclose the semiconductor article support and the pedestal. INDEPENDENT CLAIMS are included for: a) an injector as above, with a vertical column heater including a closed column surrounded by a heater, a reactant **inlet** at the bottom and a vapor **outlet** at the top, and a coupling between the vapor **outlet** and the bottom of the process **chamber**, with the vapor **outlet** being adjacent to the bottom of the process **chamber**; and b) a vertical furnace for treating a number of semiconductor articles, comprising a base, a process **container** on it, a furnace heating element on the base and with a cavity to receive the process **container**.

USE - Thermal **processing** of **semiconductor** articles such as wafers, including chemical deposition and etching. ADVANTAGE - The thermal efficiency of the reactant heating system is improved.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional elevation of a double lift vertical furnace.

Base 10

Heating element assembly 12

Outer canister 14

Resistance heating elements 16

Heater **liner** 18

Heating assembly actuators 20

Process **container** 22

Actuators 24

Pedestal 26

Semiconductor article support 28

Elongate tube 30

Discharge tube 32

Extending tube section 34

Vertical **outlet** 36

Direct section 38

Circuitous section 40

Coupling. 56

Dwg.1/3

FS EPI GMPI

FA AB; GI

MC EPI: U11-C03A; U11-C07A; U11-C09B

L165 ANSWER 7 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-139794 [18] WPIX

DNN N2002-105370

TI **Temperature controlled** gas feed-through for vaporization of liquid precursors and deposition of metal film on silicon substrate.

DC U11 X25

IN DORNFEST, C; JIN, X; KU, V; SAJOTO, T; SELYUTIN, L; ZHAO, J

PA (MATE-N) APPLIED MATERIALS INC; (DORN-I) DORNFEST C; (JINX-I) JIN X; (KUVV-I) KU V; (SAJO-I) SAJOTO T; (SELY-I) SELYUTIN L; (ZHAO-I) ZHAO

CYC 21

PI WO 2001098556 A2 20011227 (200218)* EN 63p C23C016-44

RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

W: JP KR

ADT WO 2001098556 A2 WO 2001-US19118 20010615

PRAI US 2000-595767 20000616

IC ICM C23C016-44

AB WO 200198556 A UPAB: 20020319

NOVELTY - Substrate processing system comprises a housing with a passage through it and a feed-through including a U-shaped cell, an inner wall defining the gas passage, an outer wall sealably coupled to the inner wall defining a space between the walls separated from the gas passageway and a heating element placed along the U-shaped shell. Low volatility precursors are transported in the form of liquid to a vaporizer to be converted to a vapor phase transported at elevated temperatures to prevent condensation on **chamber** components. The **chamber** contains a series of heated **temperature controlled internal liners** such as heated gas feed-through.

USE - For deposition of metal-oxide film on silicon wafers.

ADVANTAGE - Unwanted condensation or decomposition of precursors is prevented.

DESCRIPTION OF DRAWING(S) - Drawing shows a perspective view of the **chamber**.

Chemical vapor deposition system

10

Chamber body 12

Heated lid 14

Vaporizer module 16

Exhaust pumping-system. 18

Dwg.1/27

FS EPI

FA AB; GI

MC EPI: U11-C09C; U11-C09Q; X25-A04

L165 ANSWER 8 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2002-024603 [03] WPIX

DNN N2002-018981 DNC C2002-006759

TI Effluent abatement system for **semiconductor** manufacturing **process**, has thermal oxidation **reactor** to convert halogen-containing compound to a form which is more treatable at inlet end, using water vapor.

DC E16 E36 J01 L03 U11

IN ARNO, J I; VERMEULEN, R M; ARNO, J L

PA (ADTE-N) ADVANCED TECHNOLOGY MATERIALS; (ATMI-N) ATMI ECOSYS CORP

CYC 4

PI SG 80662 A1 20010522 (200203)* 45p B01D053-68

KR 2001039524 A 20010515 (200203) H01L021-02

TW 450831 A 20010821 (200239) B01D053-34

US 6423284 B1 20020723 (200254) C01B007-00

ADT SG 80662 A1 SG 1999-5667 19991115; KR 2001039524 A KR 2000-3615
20000126; TW 450831 A TW 1999-119722 19991111; US 6423284 B1 US
1999-420080 19991018

PRAI US 1999-420080 19991018

IC ICM B01D053-34; B01D053-68; C01B007-00; H01L021-02

ICS H01L021-465

AB SG 80662 A UPAB: 20020114

NOVELTY - The system (10) consists of an thermal oxidation **reactor** (12) with inlet assembly (14), provided downstream to the semiconductor manufacturing plant (79). The **reactor** raises the temperature of effluent fluid stream and treats the halogen-containing components of the effluent fluid stream using water vapor, such that a portion of components are converted to a form which is more treatable at the inlet end.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:

(1) a thermal oxidation **reactor** which has housing containing effluent gas flow passage. The inlets (89,90) are provided for the flow of shrouding gas such as nitrogen concurrently with the effluent gas and reagent gas concurrently with the shrouding gas, to the central flow passage;

(2) effluent fluid stream treating method involves injecting water vapor to inlet of **reactor**.

Subsequently the effluent fluid stream is mixed with the oxidizer medium by injecting clean dry air downstream to the inlet of **reactor**. The effluent fluid stream is heated within the predetermined temperature range. Shrouding gas is passed between water vapor and halogen containing effluent gas and introduced to gas flow path of **reactor**. The water vapor is formed in the **reactor** by combustion hydrocarbon and an oxidant.

USE - For treating effluent gas streams generated during manufacture of semiconductor materials such as VLSI and ULSI circuits, CMOS, NMOS, BiCMOS, DRAM, SRAM, FeRAM, etc.

ADVANTAGE - The halogen containing components are treated effectively. Usage of water vapor allows maximum reaction time and protects abatement system from corrosion due to early reaction. The acidic components are removed efficiently by post treatment unit. Premature reaction of products resulting in the clog of the **reactor's** inlet and formation of particulates, are prevented by using shrouding gas for separating effluent gas from water vapor. The effluent gas treatment is performed economically. The **liner** protects the **reactor** from corrosion. Desired temperature and pressure levels for the effluent abatement process can be determined, to achieve a desired level of abatement of halogen component in the effluent gas.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic representation of the effluent abatement system.

System 10

Thermal oxidation **reactor** 12

Inlet assembly 14

Liner 20

water spray **nozzles** 48

Water scrubbing unit 58

Semiconductor manufacturing plant 74

Inlets 89,90

Dwg.1/4

TECH SG 80662 A1 UPTX: 20020114

TECHNOLOGY FOCUS - MECHANICAL ENGINEERING - Preferred Apparatus: A

post treatment unit provided downstream to the **reactor** and upstream to oxidizing unit, removes the acidic components from fluid stream. The pre-treatment unit removes the water-soluble components and particulates. A vaporizing unit provides water vapor to the inlet end of **reactor**. A purge gas is also used for treating the halogen containing components. Oxygen containing gas and hydrocarbon gas are mixed at the inlet end of **reactor**. The effluent fluid stream is heated at 650-950degreesC. The **semiconductor manufacturing process** plant has high density plasma **chemical vapor deposition** tools with a remote plasma source for disassociating diatomic halogen gas from halogen containing gases during cleaning processes. Preferred **Reactor**: A **liner** (20) susceptible to corrosion, contacts the halogen species in the absence of reagent gas. The semiconductor manufacturing plant utilizes perfluoro compound as a reagent for producing effluent gas containing fluorine and/or fluorinated compounds. The effluent gas flow supply line is coupled to a water scrubbing unit (58) consisting of water spray **nozzles** (48) and quenching unit.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: The water-soluble components and particulates are removed from the effluent fluid stream, before performing oxidation and conversion. Purge gas is selected from nitrogen, clean dry air and other inert gases. The diatomic halogen is chlorine, fluorine, iodine or bromine.

FS CPI EPI
 FA AB; GI
 MC CPI: E10-H04; E11-Q02; E31-B03; J01-E02H; L04-C
 EPI: U11-C

L165 ANSWER 9 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2001-614386 [71] WPIX

TI Device and method for transferring substrate of semiconductor and lcd manufacturing device.

DC U11 U14

IN BAE, J H

PA (BAEH-I) BAE H

CYC 1

PI KR 2001025633 A 20010406 (200171)* 1p H01L021-68

ADT KR 2001025633 A KR 2001-1906 20010112

PRAI KR 2001-1906 20010112

IC ICM H01L021-68

AB KR2001025633 A UPAB: 20011203

NOVELTY - A device and a method for transferring a substrate of a semiconductor and LCD(Liquid Crystal Display) manufacturing device are provided to reduce foot print and production costs, simplify construction of a system and shorten processing time of a wafer.

DETAILED DESCRIPTION - A front-end system(200) comprises a number of load **ports**(100,102,104) loading a wafer or a LCD glass substrate, an ATM(Asynchronous Transfer Mode) robot(202) transferring the loaded wafer or the substrate in a space not

polluted at a waiting state and an ATM aligner(204) **lining** up a position of the transferred wafer or the LCD. The first and the second load lock **chamber**(300,302) respectively comprise the first and the second vacuum transfer arm(304,306) each located at a center of a main frame. The first and the second vacuum transfer arm(304,306) load the transferred wafer or the substrate on the first and the second end effect, directly transfer the loaded wafer or the substrate to the first and the second process **chamber**(504,506) and transfer the wafer or the substrate the process is ended to the first and the second end effect. The first and the second slot valve(400,402) separate the first and the second load lock **chamber**(300,302) from the first and the second process module(500,502). The first and second process module(500,502) respectively comprise the first and the second process **chamber**(504,506) to performs a **process** of the **wafer** or the substrate transferred by the first and the second load lock **chamber**(300,302).

Dwg.1/10

FS EPI
FA AB; GI
MC EPI: U11-F02A1; U14-K01A5

L165 ANSWER 10 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2001-570307 [64] WPIX

DNN N2001-425039

TI Plasma **processing** system for **semiconductor processing**, has **ceramic liner** supported between side wall of **chamber** and substrate support periphery, which is heated by radiant heater.

DC U11 V05 X14

IN KENNEDY, W S; MARASCHIN, R A; WICKER, T E

PA (LAMR-N) LAM RES CORP

CYC 95

PI WO 2001022478 A1 20010329 (200164)* EN 25p H01L021-00

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
MW MZ NL OA PT SD SE SL SZ TZ UG ZW

W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE
DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG
KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ
PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN
YU ZA ZW

AU 2000073683 A 20010424 (200164) H01L021-00

US 6227140 B1 20010508 (200164) C23C016-00

EP 1214732 A1 20020619 (200240) EN H01L021-00

R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK
NL PT RO SE SI

ADT WO 2001022478 A1 WO 2000-US24866 20000911; AU 2000073683 A AU
2000-73683 20000911; US 6227140 B1 US 1999-401308 19990923; EP
1214732 A1 EP 2000-961776 20000911, WO 2000-US24866 20000911

FDT AU 2000073683 A Based on WO 200122478; EP 1214732 A1 Based on WO
200122478

PRAI US 1999-401308 19990923

IC ICM C23C016-00; H01L021-00

AB WO 200122478 A UPAB: 20011105

NOVELTY - Vacuum **chamber** (2) has interior space (4) bounded by side walls. The substrate is supported on support (8) within interior space. Side wall is spaced outwardly from substrate support periphery. Process gas is supplied to interior space through gas pipe. Energy source ionizes the process gas in interior space. **Ceramic liner** (20) supported between wall and support periphery, is heated by radiant heater (28).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for substrate processing method.

USE - For plasma processing such as etching, **chemical vapor deposition** (CVD) on silicon substrate.

ADVANTAGE - **Ceramic liner** confines plasma inwardly and avoids attack of Al walls or other components by plasma.

DESCRIPTION OF DRAWING(S) - The figure shows the plasma reaction **chamber**.

Vacuum **chamber** 2

Interior space 4

Support 8

Ceramic liner 20

Radiant heater 28

Dwg.1/5

FS EPI

FA AB; GI

MC EPI: U11-C09C; V05-F04D1; V05-F05C; V05-F08D1; X14-F02

L165 ANSWER 11 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2001-464804 [50] WPIX

DNN N2001-344798 DNC C2001-140261

TI **Ceramic liner** for plasma processing system for **processing semiconductor** substrates, consists of ceramic tiles having interlocking edges, provided between **chamber** side wall and periphery of substrate support.

DC L03 U11 V05 X14

IN HUBACEK, J S; KENNEDY, W S; MARASCHIN, R A

PA (LAMR-N) LAM RES CORP

CYC 95

PI WO 2001022471 A1 20010329 (200150)* EN 30p H01J037-32

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC

MW MZ NL OA PT SD SE SL SZ TZ UG ZW

W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE

DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG

KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ

PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN

YU ZA ZW

AU 2000074779 A 20010424 (200150) H01J037-32

EP 1138055 A1 20011004 (200158) EN H01J037-32

R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK

NL RO SI

KR 2001080529 A 20010822 (200213) H01L021-205
 CN 1327612 A 20011219 (200226) H01J037-32
 US 6408786 B1 20020625 (200246) C23C016-507
 ADT WO 2001022471 A1 WO 2000-US24868 20000911; AU 2000074779 A AU
 2000-74779 20000911; EP 1138055 A1 EP 2000-963352 20000911, WO
 2000-US24868 20000911; KR 2001080529 A KR 2001-706436 20010522; CN
 1327612 A CN 2000-802344 20000911; US 6408786 B1 US 1999-401193
 19990923
 FDT AU 2000074779 A Based on WO 200122471; EP 1138055 A1 Based on WO
 200122471
 PRAI US 1999-401193 19990923
 IC ICM C23C016-507; H01J037-32; H01L021-205
 ICS C23C016-50
 AB WO 200122471 A UPAB: 20010905
 NOVELTY - **Ceramic liner** which is held between
chamber side wall and periphery of substrate support, has
 ceramic tiles (34) having interlocking edges. Each ceramic tile is
 attached to respective metal backing plate (36) fixed to thermally
 controlled block via bendable metal frame (40). An elastomeric joint
 attaches ceramic tile to metal backing plate.
 DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included
 for substrate processing method in which the substrate is etched
 with plasma produced in the **chamber**.
 USE - The **ceramic liner** is used in a plasma
 processing system used for **processing**
semiconductor substrates (claimed).
 ADVANTAGE - **Ceramic liner** and other
 components are compatible to plasma surrounding. The heating or
 cooling of **liner** is easy because it has high thermal
 conductivity. The contamination of aluminum walls or components, is
 prevented due to provision of **ceramic liner**.
 DESCRIPTION OF DRAWING(S) - The figure shows perspective view
 of **ceramic liner**.
 Ceramic tiles 34
 Metal backing plate 36
 Bendable metal frame 40
 Dwg.3/7
 FS CPI EPI
 FA AB; GI
 MC CPI: L04-D04
 EPI: U11-C09C; V05-F04D1; V05-F05C; X14-F02

 L165 ANSWER 12 OF 42 WPIX (C) 2002 THOMSON DERWENT
 AN 2001-331774 [35] WPIX
 DNN N2001-239017 DNC C2001-102547
 TI Plasma processing device for e.g. **etching** of
semiconductor, has metallic or **ceramic** made gate
liner detachably provided in **chamber** gate.
 DC L03 U11 X14
 PA (TKEL) TOKYO ELECTRON LTD
 CYC 2
 PI JP 2001077088 A 20010323 (200135)* 7p H01L021-3065

KR 2001030159 A 20010416 (200163) H01L021-18
ADT JP 2001077088 A JP 1999-248299 19990902; KR 2001030159 A KR
2000-50635 20000830
PRAI JP 1999-248299 19990902
IC ICM H01L021-18; H01L021-3065
ICS C23C016-505; H01L021-205; H05H001-46
AB JP2001077088 A UPAB: 20010625
NOVELTY - A **chamber** gate (22) for introducing and taking
out a workpiece is formed on a side wall of a vacuum **chamber**
(1). A metallic or **ceramic** made gate **liner** (24)
is detachably provided in the **chamber** gate.
USE - For plasma etching, film forming, etc.
ADVANTAGE - Prevents damage of **chamber** gate by
deposition or sputtering due to provision of gate **liner**.
DESCRIPTION OF DRAWING(S) - The figure shows the perspective
cross sectional view of the plasma processing device. (Drawing
includes non-English language text).
Vacuum **chamber** 1
Chamber gate 22
Gate **liner** 24
Dwg.1/6
FS CPI EPI
FA AB; GI
MC CPI: L04-C07D
EPI: U11-C01B; U11-C07A1; X14-F

L165 ANSWER 13 OF 42 WPIX (C) 2002 THOMSON DERWENT
AN 2001-138397 [14] WPIX
DNN N2001-100696 DNC C2001-040880
TI Process for **etching** substrates in **semiconductor**
processing including dissociation of etchant using plasma.
DC L03 U11 V05
IN PODLESNIK, D; QIAN, X; SUN, Z; XU, S
PA (MATE-N) APPLIED MATERIALS INC
CYC 27
PI WO 2001004927 A2 20010118 (200114)* EN 33p H01J037-32
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR
EP 1198822 A2 20020424 (200235) EN H01J037-32
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK
NL PT RO SE SI
ADT WO 2001004927 A2 WO 2000-US19152 20000712; EP 1198822 A2 EP
2000-947339 20000712, WO 2000-US19152 20000712
FDT EP 1198822 A2 Based on WO 200104927
PRAI US 1999-352008 19990712
IC ICM H01J037-32
ICS H01L021-02
AB WO 200104927 A UPAB: 20010312
NOVELTY - Process comprises introducing etchant into **chamber**
(10) and striking plasma in **chamber** to minimise deposition
of material on the inner surface of the **chamber**. The
recombination rate of the disassociated etchant on the material is

different to the recombination rate of the etchant on the inner surface.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) a process for etching a substrate where a 1st and 2nd etchant are used, the volumetric flow of the 1st being more than that of the 2nd and the deposition rate of the disassociated 1st etchant being more than that of the disassociated 2nd etchant;

(2) a process for etching substrates in a **chamber** where the 1st substrate is etched at a 1st pressure according to a main etch recipe, then etching at a 2nd smaller pressure (ca. 30 mTorr less) according to an overetch recipe;

(3) process for etching a substrate comprising flowing chemical mixture into **chamber** housing substrate, striking plasma in **chamber** to form one or more plasma constituents and depositing film on inner surface;

(4) a process for etching a substrate in a **chamber** where the chemical mixture comprises a bromine-containing fluid and/or a chlorine-containing fluid together with a fluorine-containing fluid; and

(5) an apparatus for etching a substrate comprising a process **chamber**, one or more sources of etchants coupled to the process **chamber** and at least one coil next to the process **chamber** to strike a plasma.

USE - **Semiconductor processing.**

ADVANTAGE - The process and apparatus minimises process sensitivity to **chamber** conditions during etching processes.

DESCRIPTION OF DRAWING(S) - The diagram shows a schematic view of an etching **chamber**.

Chamber 10

Electrically grounded body 12

Dome ceiling 13

Plasma zone 14

Support member 16

Substrate 20

Gas distributor 22

Inductor coil 26

Coil power supply 27

Electrode power supply 28

Exhaust system 30

Throttle valve 32

Exhaust **port** 34

Dwg.1/10

TECH WO 200104927 A2UPTX: 20010312

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Process: The deposition rate of material on the inner surface is less than 40 Angstroms/minute. The inner surface is cleaned before the etching process starts. Oxygen is flown into the **chamber**. The overetch recipe comprises flowing one or more of a bromine-containing fluid, a chlorine-containing fluid or a mixture into the **chamber**, preferably a bromine-containing fluid or

chlorine-containing fluid and an oxygen-containing fluid.
 Preferred Etchant: The 1st etchant comprises chlorine (Cl) and the 2nd etchant comprises bromine (Br). Preferably the fluorine-containing fluid comprises one or more of SF₆, NF₃ or a mixture with the volumetric flow being less than 20% of the chemical mixture, or CF₄ and O₂ with volumetric flow being less than 50% and the volumetric flow ratio of CF₄ to O₂ being 4:1, or CF₄ with the volumetric flow being less than 50% of the chemical mixture.

Preferred Substrate: The substrate comprises silicon (Si).

Preferred Apparatus: The internal surface is made of quartz and comprises a **liner** disposed on a **chamber** body.

FS CPI EPI

FA AB; GI

MC CPI: L04-C07

EPI: U11-C09B; U11-C09C; U11-C09F; V05-F05C; V05-F08D1; V05-F08E1

L165 ANSWER 14 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2001-091692 [10] WPIX

DNN N2001-069437 DNC C2001-027099

TI Coating metallic surface of plasma **chamber** sidewall used in **semiconductor processing**, by electroless plating phosphorus nickel and plasma spraying ceramic coating.

DC L02 L03 M13 U11 V05 X14

IN CHANG, C; STEGER, R; STEGER, R J

PA (LAMR-N) LAM RES CORP

CYC 93

PI WO 2001000901 A1 20010104 (200110)* EN 18p C23C028-00

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
 MW MZ NL OA PT SD SE SL SZ TZ UG ZW

W: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK
 DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
 KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL
 PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU
 ZA ZW

AU 2000065407 A 20010131 (200124) C23C028-00

US 6444083 B1 20020903 (200260) H01L021-302

ADT WO 2001000901 A1 WO 2000-US40229 20000614; AU 2000065407 A AU
 2000-65407 20000614; US 6444083 B1 US 1999-343692 19990630

FDT AU 2000065407 A Based on WO 200100901

PRAI US 1999-343692 19990630

IC ICM C23C028-00; H01L021-302

ICS C23C016-00; C23C018-36; C23F001-02

AB WO 200100901 A UPAB: 20010220

NOVELTY - A metal surface of a component of **semiconductor processing** equipment is coated by depositing phosphorus nickel plating on the metal surface, and depositing ceramic coating on the phosphorus nickel plating. The ceramic coating forms an outermost surface.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a component of **semiconductor processing** equipment.

USE - For coating a metal surface of a component of

semiconductor processing equipment, e.g. parts of plasma processing **reactor chamber**. The components include **chamber** walls, substrate supports, gas distribution systems including showerheads, baffles, rings, **nozzles**, fasteners, heating elements, plasma screens, **liners**, and transport module components, e.g. robotic arms, and inner and outer **chamber** walls.

ADVANTAGE - Provides an effective way to provide corrosion resistance to metal surfaces of components of **semiconductor processing** apparatus. Unsatisfactory etching of undesirable formation of pinholes in deposited films is reduced by suppressing occurrence of dust by corrosion.

Dwg.0/2

TECH WO 200100901 A1UPTX: 20010220

TECHNOLOGY FOCUS - METALLURGY - Preferred Method: The phosphorus nickel plating is deposited to a thickness of 0.002-0.004 inches, by electroless plating. It is subjected to a surface roughening treatment before depositing the ceramic coating. The metal surface is anodized or unanodized aluminum or aluminum alloy. The nickel plating consists of 9-12 wt.% phosphorus.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Method: The ceramic coating is deposited on the roughened phosphorus nickel plating by plasma spraying. The ceramic coating is silicon carbide, silicon nitride, boron carbide, aluminum nitride, or preferably alumina. The ceramic coating has a thickness of 0.005-0.040, preferably 0.005-0.030 inches.

FS CPI EPI

FA AB

MC CPI: L02-A06; L02-G11; L02-H02A; L02-H02B2; L02-J01E; L04-D01; L04-D04; M13-B

EPI: U11-C09A; U11-C09C; V05-F04D1; V05-F04G; V05-F05C; V05-F08D1; V05-F08E1; V05-L03A; V05-L03B; V05-L05F5; X14-F02

L165 ANSWER 15 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2001-070100 [08] WPIX

DNN N2001-052999 DNC C2001-019469

TI Chemical deposition system useful for cleaning **chemical vapor deposition chambers** includes a cleaning **process wafer** loaded to a wafer support.

DC L03 U11

IN GUPTA, A; MURUGESH, L; PONNEKANTI, S; RIMPLE, G A

PA (MATE-N) APPLIED MATERIALS INC

CYC 1

PI US 6159333 A 20001212 (200108)* 7p C23F001-02

ADT US 6159333 A US 1998-169058 19981008

PRAI US 1998-169058 19981008

IC ICM C23F001-02

AB US 6159333 A UPAB: 20010207

NOVELTY - A chemical deposition system includes a cleaning **process wafer** which is loaded to a wafer support.

The cleaning **process wafer** has a dielectric constant, which spreads plasma formed from a cleaning agent by a plasma-generating system.

DETAILED DESCRIPTION - A chemical deposition system (10) configurable to clean its processing **chamber** comprises a wafer support (12) mounted in the processing **chamber**, a gas discharge head for introducing a cleaning agent into the **chamber**, a plasma-generating system, and a cleaning **process wafer** (40) adapted for loading to the wafer support. The cleaning **process wafer** has a dielectric constant, which spreads plasma formed from the cleaning agent by the plasma-generating system when it is on the wafer support. An INDEPENDENT CLAIM is also included for a memory (45) storing program for access by a processor (43) to control the chemical deposition system comprising an instruction for removing the **process wafer** from the **processing chamber**, an instruction for loading the cleaning **process wafer** to a susceptor in the **processing chamber**, an instruction for flowing the cleaning agent into the **processing chamber**, and an instruction for forming a plasma from the cleaning agent in the **processing chamber**.

USE - For cleaning **chemical vapor deposition chambers**.

ADVANTAGE - The inventive chemical deposition system allows reduction of plasma cleaning time while protecting the wafer support during cleaning operation. It also allows for an increase lifetime of the wafer support, thus reducing maintenance costs and downtime of substrate processing system and increasing wafer throughput.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional diagram of a **processing chamber** including the wafer.

Chemical deposition system 10

Wafer support 12

Cleaning **process wafer** 40

Processor 43

Memory 45

Dwg.1/3

TECH US 6159333 A UPTX: 20010207

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The wafer support is a susceptor comprising an anodized aluminum. The cleaning **process wafer** comprises alumina (AL₂O₃). Preferred Property: The cleaning **process wafer** is 40 mils thick.

TECHNOLOGY FOCUS - MECHANICAL ENGINEERING - The chemical deposition system further includes a wafer elevator having slots for holding wafers including the cleaning **process wafer**, and a robot arm for moving the cleaning **process wafer** between the susceptor and the wafer elevator. The **chamber** includes walls lined with a **ceramic liner**. The cleaning **process wafer** directs the plasma formed in the **chamber** towards the walls of the **chamber**.

FS CPI EPI
 FA AB; GI
 MC CPI: L04-D01; L04-D10
 EPI: U11-C09B; U11-C09C; U11-C09F; U11-F02A2

L165 ANSWER 16 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2000-637996 [61] WPIX

DNN N2000-473217 DNC C2000-191828

TI Metal line deposition in semiconductor device manufacture is started when wafer is at a first temperature and continued while heating to a higher, target temperature.

DC L03 U11

IN CLEVENGER, L; IGGULDEN, R; SCHMIDBAUER, S; WEBER, S J; WEIGAND, P

PA (SIEI) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBM) INT BUSINESS MACHINES CORP

CYC 22

PI US 6136709 A 20001024 (200061)* 10p H01L021-24
 WO 2001026148 A1 20010412 (200123) EN H01L021-768
 RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
 W: CN JP KR

ADT US 6136709 A US 1999-413265 19991006; WO 2001026148 A1 WO 2000-US27145 20001002

PRAI US 1999-413265 19991006

IC ICM H01L021-24; H01L021-768

ICS H01L021-4763

AB US 6136709 A UPAB: 20001128

NOVELTY - Semiconductor wafer having dielectric layer with vias is placed in a **chamber** for deposition of metal to fill the vias. Deposition is started when wafer is at a first temperature and continued while heating to a higher, target **temperature**. **Control** of an intermediate temperature between above two temperatures is achieved by programming a thermal gradient in thermal surface on which wafer is mounted.

DETAILED DESCRIPTION - The metal may include one of tungsten, gold and copper. When the metal includes aluminum, the first temperature is about 150 deg. C and target temperature is about 350 deg. C.

Metal deposition is completed in less than 110 seconds, and the metal deposited on the semiconductor **wafer** is subsequently **etched** to form metal lines.

The thermal gradient can be non-linear, linear or exponential.

INDEPENDENT CLAIMS are given for depositing metal lines and contacts for semiconductor devices.

USE - Formation of metal lines used to interconnect components on semiconductor devices.

ADVANTAGE - Shorter process time resulting in higher throughput. Reduced contact resistance and increased electromigration lifetime.

DESCRIPTION OF DRAWING(S) - The drawing shows a partial cross-sectional view of a wafer with the metal patterned in accordance with the invention.

Target layer 200

Wafer 201
 Dielectric layer 202
 Target conductor 203
 Metal **liner** 207
 Contacts 212
 Metal lines 214
 Dwg.5/5
 FS CPI EPI
 FA AB; GI
 MC CPI: L04-C10A; L04-C13B
 EPI: U11-C05C5; U11-C05D3; U11-C05G2C

L165 ANSWER 17 OF 42 WPIX (C) 2002 THOMSON DERWENT
 AN 2000-595693 [57] WPIX
 CR 1996-261632 [27]; 1997-322161 [30]
 DNN N2000-441242 DNC C2000-178094
 TI **CVD processing chamber** for
 semiconductor fabrication has inner **ceramic**
 lining to prevent wall next to processing location being
 exposed to plasma.
 DC L03 U11
 IN CHO, T; DORNFEST, C; FAIRBAIRN, K; GUO, X S; SCHREIBER, A; WHITE, J
 M; WOLFF, S; ZHAO, J
 PA (MATE-N) APPLIED MATERIALS INC
 CYC 5
 PI EP 1041171 A1 20001004 (200057)* EN 32p C23C016-44
 R: DE FR GB IT NL
 ADT EP 1041171 A1 Div ex EP 1995-117865 19951113, EP 2000-114451
 19951113
 FDT EP 1041171 A1 Div ex EP 714998
 PRAI US 1994-348273 19941130
 IC ICM C23C016-44
 AB EP 1041171 A UPAB: 20001205

NOVELTY - **CVD** apparatus comprises vacuum processing
chamber (133), substrate support and gas inlet. The
chamber includes openings to a vacuum duct which is
 connected to a vacuum system. The **chamber** has an inner
ceramic lining to prevent wall next to processing
 location being exposed to plasma.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the
 method of protecting the walls of the **chamber**. Energized
 gas distribution face plate (122) is located opposite substrate
 pedestal (136) and is electrically earthed. The walls of the
chamber are lined with a removable **ceramic**
ring lining.

USE - Apparatus for **chemical vapor**
deposition in semiconductor fabrication.

ADVANTAGE - The **ceramic lining** prevents the
 formation of a layer of material on the **chamber** wall.
 Such a deposit can break off and cause defects to form on the
 surface being coated.

DESCRIPTION OF DRAWING(S) - The figure shows the processing

chamber.

Gas distribution face plate 122

Processing **chamber** 133

Pedestal 136

Dwg.2/23

FS CPI EPI

FA AB; GI

MC CPI: L04-D01

EPI: U11-C09B

L165 ANSWER 18 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2000-442405 [38] WPIX

DNN N2000-330087 DNC C2000-134567

TI High temperature **chemical vapor deposition chamber** for wafer

processing comprises a heated inside **liner** and a **temperature-controlled** outer **chamber** body.

DC L03 U11

IN CHEN, J J; CHIAO, S H; HUSTON, J; LEI, L C; NGUYEN, A N; UMOTOY, S P; VO, B V

PA (CHEN-I) CHEN J J; (CHIA-I) CHIAO S H; (HUST-I) HUSTON J; (LEIL-I) LEI L C; (NGUY-I) NGUYEN A N; (UMOT-I) UMOTOY S P; (VOBV-I) VO B V; (MATE-N) APPLIED MATERIALS INC

CYC 5

PI WO 2000036179 A2 20000622 (200038)* EN 47p C23C016-00
W: CN JP KR

US 2001054381 A1 20011227 (200206) C23C016-00

KR 2001080758 A 20010822 (200213) C23C016-00

TW 447014 A 20010721 (200219) H01L021-205

US 6364954 B2 20020402 (200226) C23C016-00

ADT WO 2000036179 A2 WO 1999-US29115 19991207; US 2001054381 A1 US 1998-211998 19981214; KR 2001080758 A KR 2001-707351 20010613; TW 447014 A TW 1999-120548 19991124; US 6364954 B2 US 1998-211998 19981214

PRAI US 1998-211998 19981214

IC ICM C23C016-00; H01L021-205

ICS H01L021-44

AB WO 200036179 A UPAB: 20000811

NOVELTY - A high temperature **chemical vapor deposition (CVD) chamber** (100) comprises

a **liner** (200) enclosed in a **chamber** body (250).

The **liner** is maintained at a first temperature (T1) and the body is maintained at a second temperature (T2), which is lower than T1.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of **wafer processing** comprising heating a pedestal to T3, maintaining a **liner** at T1 and a **chamber** at T2, and injecting process gases into the **chamber** for film deposition, in which T3 is greater than T1, and T1 is greater than T2.

USE - For **wafer processing**, e.g. deposition

of titanium nitride film by thermal reaction between titanium tetrachloride and ammonia (claimed).

ADVANTAGE - The CVD chamber has a heated liner which maintains a spaced apart distance from the chamber body so that the liner is maintained at a higher temperature than the chamber body. The liner can be maintained at a temperature that reduces the amount of deposition on the liner while maintaining a safe temperature for the chamber body.

DESCRIPTION OF DRAWING(S) - The figure shows a partial cross-sectional perspective view of a high temperature chemical vapor deposition chamber.

Pedestal 180

Liner 200

Body 250

Base 252

Showerhead 300

Exhaust assembly 600

Dwg.1/7

TECH WO 200036179 A2UPTX: 20000811

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The pins are made of stainless steel or nickel.

Preferred Parameters: T1 is approximately 150-250degreesC and T2 is approximately 60-65degreesC. The pedestal is maintained at a third temperature (T3) approximately 600-800degreesC. T4 is approximately 150-200degreesC.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Materials: The pedestal is made of a ceramic material (preferably aluminum nitride).

ABEX WO 200036179 A2UPTX: 20000811

EXAMPLE - In an EMBODIMENT of the invention, the liner and the body are separated from one another by pins. The liner further comprises a heater. A pedestal (180) is positioned centrally within the liner to support a substrate within the chamber. An exhaust assembly (600) is connected to the chamber body and at least one heater is positioned proximate the exhaust assembly to maintain the assembly at T4. The chamber further comprises an annular edge ring, a shaft-like portion, and a showerhead (300). The chamber body has a chamber side and an annular-shaped chamber base (252).

FS CPI EPI

FA AB; GI

MC CPI: L04-D01

EPI: U11-C03A; U11-C09B

L165 ANSWER 19 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 2000-303505 [26] WPIX

CR 1999-591414 [50]

DNN N2000-226771 DNC C2000-092089

TI Plasma processing chamber for use during processing of semiconductor wafers has a

chamber liner and a **liner** support including a flexible wall surrounding the **liner's** external surface.

DC L03 U11 V05 X14
IN KENNEDY, W S; MARASCHIN, R A; WICKER, T E
PA (LAMR-N) LAM RES CORP; (KENN-I) KENNEDY W S; (MARA-I) MARASCHIN R A;
(WICK-I) WICKER T E

CYC 91

PI WO 2000019481 A2 20000406 (200026)* EN 39p H01J037-00
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM
EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ
LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD
SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

AU 2000014401 A 20000417 (200035) H01J037-00
US 6129808 A 20001010 (200052) H05H001-00
EP 1145273 A2 20011017 (200169) EN H01J037-00
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
KR 2001075264 A 20010809 (200211) H01L021-3065
CN 1319247 A 20011024 (200213) H01J037-00
US 6394026 B1 20020528 (200243) C23C016-507
TW 460972 A 20011021 (200248) H01L021-3065
US 2002102858 A1 20020801 (200253) H01L021-302

ADT WO 2000019481 A2 WO 1999-US20890 19990924; AU 2000014401 A AU
2000-14401 19990924; US 6129808 A CIP of US 1998-50902 19980331, US
1998-161074 19980925; EP 1145273 A2 EP 1999-969835 19990924, WO
1999-US20890 19990924; KR 2001075264 A KR 2001-703624 20010321; CN
1319247 A CN 1999-811286 19990924; US 6394026 B1 CIP of US
1998-50902 19980331, Cont of US 1998-161074 19980925, US 2000-487325
20000119; TW 460972 A TW 1999-116512 19990927; US 2002102858 A1 CIP
of US 1998-50902 19980331, Cont of US 1998-161074 19980925, Div ex
US 2000-487325 20000119, US 2002-101737 20020321

FDT AU 2000014401 A Based on WO 200019481; EP 1145273 A2 Based on WO
200019481; US 6394026 B1 Cont of US 6129808; US 2002102858 A1 Cont
of US 6129808, Div ex US 6394026

PRAI US 1998-161074 19980925; US 1998-50902 19980331; US 2000-487325
20000119; US 2002-101737 20020321

IC ICM C23C016-507; H01J037-00; H01L021-302; H01L021-3065; H05H001-00

AB WO 200019481 A UPAB: 20020820

NOVELTY - A plasma processing **chamber** (100) has a **chamber liner** (130) and a **liner** support (134) which includes a flexible wall (134b) configured to surround an external surface of the **liner**. The flexible wall is spaced apart from the **chamber liner's** wall.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of **processing** a **semiconductor** substrate in the plasma processing **chamber**, where a semiconductor wafer is transferred into the **chamber** and an exposed surface of the substrate is processed with a high density plasma.

USE - For use during **processing** of

semiconductor wafers, i.e., to receive processing gases while a radio frequency (RF) power is applied to processing **chamber's** electrode(s).

ADVANTAGE - The plasma etching **chamber** has **lining** materials that reduce particle and metallic contamination during processing. It has consumable parts which are more resistant to erosion and can withstand temperature variations while preventing damage.

DESCRIPTION OF DRAWING(S) - The figure shows a high density plasma etching **chamber**.

High density plasma etching **chamber** 100

Chamber liner 130

Baffle ring 132

Liner support 134

Flexible wall 134b

Dwg.1/8

TECH WO 200019481 A2UPTX: 20000531

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The **liner** support is made from a flexible aluminum material and the **chamber liner** comprises a **ceramic**

material. The baffle ring and **chamber liner** are

each made from silicon carbide (SiC), silicon nitride (Si₃N₄), boron carbide (B₄C) or boron nitride (BN).

TECHNOLOGY FOCUS - ELECTRONICS - Preferred **Chamber**: The plasma processing **chamber** further includes a baffle ring (132) in thermal contact with **chamber liner** and support. The ring defines a plasma screen around an electrostatic chuck in the central portion of the **chamber**.

FS CPI EPI

FA AB; GI

MC CPI: L03-H04D; L04-C07D; L04-D04

EPI: U11-C09C; U11-F02A2; V05-F04D1; V05-F05C; X14-F02

DRN 1247-U

L165 ANSWER 20 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1999-287897 [24] WPIX

CR 1999-277467 [23]; 1999-312454 [26]

DNN N1999-215020 DNC C1999-085047

TI Semiconductor manufacturing system.

DC E36 J01 L03 S02 S03 U11 X25

IN APPLEGARTH, C H; LORIMER, D H

PA (SAES) SAES PURE GAS INC

CYC 25

PI WO 9919049 A2 19990422 (199927)* EN 24p B01D053-04

RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

W: CN JP KR RU SG

US 6156105 A 20001205 (200066) B01D053-04

TW 393679 A 20000611 (200108) H01L021-00

US 6232204 B1 20010515 (200129) H01L021-322

ADT WO 9919049 A2 WO 1998-US21071 19981006; US 6156105 A Provisional US 1997-62043P 19971015, Provisional US 1997-62122P 19971015, Cont of

US 1997-950929 19971015, US 1999-335801 19990617; TW 393679 A TW
 1998-116865 19981222; US 6232204 B1 Provisional US 1997-62043P
 19971015, Provisional US 1997-62122P 19971015, Div ex US 1997-950929
 19971015, US 1999-252023 19990216

FDT US 6156105 A WO 9919050, Cont of US 6068685; US 6232204 B1 WO
 9919050, Div ex US 6068685

PRAI US 1997-62122P 19971015; US 1997-62043P 19971015; US 1997-950929
 19971015; US 1999-335801 19990617; US 1999-252023 19990216

IC ICM B01D053-04; H01L021-00; H01L021-322

AB WO 9919049 A UPAB: 20011105

NOVELTY - A semiconductor manufacturing system comprises a
 getter-based gas purifier with a safety device coupled in flow
 communications with a gas distribution network for a semiconductor
 fabrication facility which supplies purified gas to at least 1
wafer processing chamber. The gas

purifier comprises a getter column having a gas **inlet**
 blocking device which has a sacrificial getter bed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for
 (A) the getter column comprising (i) a **vessel** having an
inlet, an **outlet**, and a containment wall extending
 between the **inlet** and the **outlet**; (ii) a primary
 getter bed for purifying a gas within the **vessel**; and
 (iii) a gas **inlet** blocking device between the
inlet and the primary getter bed which prevents substantial
 amounts of high impurity concentration gas from flowing into the
 primary getter bed; and (B) a method of making an integrated circuit
 device by purifying a gas, supplying to at least 1 **wafer**
processing chamber and **processing** the
wafer.

USE - Used to prevent the use of impure gases in the production
 of semiconductor and integrated circuit devices.

ADVANTAGE - The safety device protects against breach of
 containment of the getter material when high concentrations of
 impurity are introduced into a getter column. The sacrificial getter
 bed melts when high impurity gas flows generating a liquid which
 blocks the flow of the gas through a porous member to prevent the
 impure gas reaching the primary getter bed. This automatically shuts
 off the flow of high impurity gas into the primary getter bed and so
 prevents damage to the primary getter bed.

DESCRIPTION OF DRAWING(S) - Figure 2A shows a cross-sectional
 view of a getter column including a gas **inlet** blocking
 device.

Getter Column 20

Gas **Inlet** Blocking Device 22

Vessel 24

Inlet 26

Outlet 28

Primary Getter Bed 32

Porous Bed Support 34

Cylindrical Housing 36

Porous Metallic Support 38

Recess in Support 38a

Sacrificial Getter Bed 40
Liner 42

Screen 44

Dwg. 2A/5

TECH WO 9919049 A2 UPTX: 19990624

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Column: The gas inlet blocking device comprises a cylindrical housing having an upper end and a lower end, a porous metallic support at the lower end and a sacrificial getter bed disposed over the support. Also, there is a high melting point, nonmetallic liner that separates the getter bed from the housing. Alternatively, the gas inlet blocking device comprises a cylindrical housing having an upper end and a lower end, a porous ceramic support at the lower end, a layer of a meltable material over the porous ceramic support and a sacrificial getter bed over the layer of meltable material. Specifically, the layer of meltable material comprises stainless steel shot.

FS CPI EPI

FA AB; GI

MC CPI: J01-E; L04-C18; L04-D10

EPI: U11-A12; U11-C09X

L165 ANSWER 21 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1999-277467 [23] WPIX

CR 1999-287897 [27]; 1999-312454 [26]

DNN N1999-207977 DNC C1999-081553

TI Getter-based gas purification system for semiconductor wafer processing.

DC J01 L03 U11

IN APPLGARTH, C H; LORIMER, D H

PA (SAES) SAES PURE GAS INC; (SAES-N) SAES PURE GAS INC

CYC 25

PI WO 9919048 A1 19990422 (199923)* EN 47p B01D053-04
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR RU SG

US 6068685 A 20000530 (200033) B01D053-04

EP 1028797 A1 20000823 (200041) EN B01D053-04

R: BE DE ES FR GB IE IT NL SE

CN 1276741 A 20001213 (200118) B01D053-04

KR 2001031096 A 20010416 (200163) H01L021-00

JP 2001519229 W 20011023 (200202) 81p B01D053-04

TW 446992 A 20010721 (200219) H01L021-00

US 6398846 B1 20020604 (200242) B01D053-04

ADT WO 9919048 A1 WO 1998-US21030 19981002; US 6068685 A US 1997-950929 19971015; EP 1028797 A1 EP 1998-952101 19981002, WO 1998-US21030 19981002; CN 1276741 A CN 1998-810257 19981002; KR 2001031096 A KR 2000-703962 20000412; JP 2001519229 W WO 1998-US21030 19981002, JP 2000-515674 19981002; TW 446992 A TW 1998-116866 19981223; US 6398846 B1 Div ex US 1997-950929 19971015, Div ex US 1999-252023 19990216, US 2000-708985 20001107

FDT EP 1028797 A1 Based on WO 9919048; JP 2001519229 W Based on WO 9919048; US 6398846 B1 Div ex US 6068685, Div ex US 6232204

PRAI US 1997-950929 19971015; US 1999-252023 19990216; US 2000-708985
20001107

IC ICM B01D053-04; H01L021-00
ICS C23C016-44; C30B025-14; H01L021-205

AB WO 9919048 A UPAB: 20020704

NOVELTY - A semiconductor manufacturing system comprises a getter-based gas purifier coupled in flow communication with a gas distribution network for a semiconductor fabrication facility. The gas purifier comprises a getter column having a metallic **vessel** with an **inlet**, an **outlet**, and a containment wall extending between the **inlet** and the **outlet**.

DETAILED DESCRIPTION - A getter material is disposed in the **vessel** with two temperature sensors, e.g. thermocouples, disposed in top and bottom portions of the getter material, respectively. Both sensors are located in a melt zone. Two high melting point nonmetallic **liners** are disposed in the **vessel** so at least some of the top and bottom portions of the getter material, respectively, are separated from the containment wall of the **vessel**. The getter column further includes: a porous support member comprised of a stainless steel plate supporting the getter material, and a barrier material comprised of stainless steel shot separating the getter material from the support member; a control unit coupled to the two temperature sensors which actuates an isolation valve to isolate the getter column when a first alarm temperature is measured, and a vent valve to vent gas from the getter column when a second alarm temperature is sensed. The purified gas from the getter column is supplied to a **semiconductor wafer processing chamber** to obtain an integrated circuit device.

USE - A getter-based gas purifier system for the supply of purified gas to a semiconductor integrated circuit manufacturing system.

ADVANTAGE - Sensors rapidly detect against breach of containment of the getter material in the event high concentrations of impurities are introduced into the getter column, and to protect the system from catastrophic failure.

Dwg.1/9

TECH WO 9919048 A1 UPTX: 19990616

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - The high melting point, nonmetallic **liners** are comprised of a material selected from quartz, zirconia (Zr2O5), SiC, SiN, and Al2O3.

ABEX WO 9919048 A1 UPTX: 19990616

EXAMPLE - Semiconductor manufacturing system (1) includes getter-based gas purifier (2) for purifying a noble gas, e.g. Ar, He, to an ultrapure level. Semiconductor fabrication facility (3) includes gas distribution network (4) for supplying gas to wafer processing chambers (5a,5b,5c,5d,5e). Gas distribution network (4) is in flow communication with an outlet for purified gas of gas purifier (2) and sources of other processing gases, e.g. N2, O2, H2. The purified gas is used to process semiconductor wafer (W) in one

or more of the processing chambers.

FS CPI EPI

FA AB; GI

MC CPI: J01-E02; L04-C18; L04-D10

EPI: U11-A12

L165 ANSWER 22 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1999-244442 [20] WPIX

DNN N1999-181896 DNC C1999-071416

TI **Chemical vapor deposition** apparatus
with a **chamber** inner lining.

DC L03 M13 U11

IN CARLSON, D K; COMITA, P B; KLINCK, K E; MELLEN, H J; COMITA, P

PA (MATE-N) APPLIED MATERIALS INC

CYC 22

PI WO 9915712 A1 19990401 (199920)* EN 20p C23C016-44

RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

W: JP KR SG

US 5914050 A 19990622 (199931) C23C016-00

EP 1017877 A1 20000712 (200036) EN C23C016-44

R: DE FR GB IT NL

JP 2001517736 W 20011009 (200174) 19p C23C016-44

ADT WO 9915712 A1 WO 1998-US18790 19980909; US 5914050 A US 1997-934920
19970922; EP 1017877 A1 EP 1998-945991 19980909, WO 1998-US18790
19980909; JP 2001517736 W WO 1998-US18790 19980909, JP 2000-512998
19980909

FDT EP 1017877 A1 Based on WO 9915712; JP 2001517736 W Based on WO
9915712

PRAI US 1997-934920 19970922

IC ICM C23C016-00; C23C016-44

ICS H01L021-205

AB WO 9915712 A UPAB: 19990525

NOVELTY - **Chemical vapor deposition**

apparatus with a **chamber** inner lining includes a
purge channel for contaminant gases etc. formed between the inner
lining and the **chamber** wall.

DETAILED DESCRIPTION - A **chemical vapor
deposition** apparatus includes: a **chamber** with an
internal **liner**; a purge channel formed between the
liner and the **chamber** wall; and **inlet**
and **outlet ports** for the purge channel.

Preferred Features: Preferably the **chamber** includes a
base ring and first and second sealing members on opposite sides of
the ring, the **liner** being a ring which lines the base
ring.

USE - In clearing material such as contaminant gases from
between an inner wall of a **chemical vapor
deposition** (CVD) **chamber** and an outer
surface of a **chamber liner**.

DESCRIPTION OF DRAWING(S) - The drawing shows a CVD
apparatus of the invention

CVD chamber 12

Base ring 18
 Inlet port 28
 Outlet port 30
 lower liner ring 44

Purge channel 46
 Dwg. 8/8

FS CPI EPI
 FA AB; GI
 MC CPI: L04-D01; M13-E07
 EPI: U11-C09B

L165 ANSWER 23 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1998-482977 [42] WPIX

DNC C1998-146203

TI Processing apparatus for use in e.g. physical vapour deposition - comprises shield for **lining** portion of interior of vacuum processing **chamber**, with heater element in shield passage.

DC M13

IN BLACK, R; DEMARAY, E; TURNER, N L

PA (KOMA-N) APPLIED KOMATSU TECHNOLOGY INC; (KOMA-N) APPLIED KOMATSU TECHNOLOGY KK; (BLAC-I) BLACK R; (DEMA-I) DEMARAY E; (TURN-I) TURNER N L

CYC 27

PI EP 866146 A1 19980923 (199842)* EN 12p C23C014-56
 R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL
 PT RO SE SI

JP 10310861 A 19981124 (199906) 38p C23C014-00

KR 98080335 A 19981125 (200004) H01L021-20

US 6432203 B1 20020813 (200255) B05C011-11

US 2002108571 A1 20020815 (200256) C23C014-32

ADT EP 866146 A1 EP 1998-301788 19980311; JP 10310861 A JP 1998-110028 19980317; KR 98080335 A KR 1998-8933 19980317; US 6432203 B1 Cont of US 1997-819599 19970317, US 1998-328503 19980109; US 2002108571 A1 Cont of US 1997-819599 19970317, Div ex US 1998-328503 19980109, US 2001-11590 20011106

PRAI US 1997-819599 19970317; US 1998-328503 19980109; US 2001-11590 20011106

IC ICM B05C011-11; C23C014-00; C23C014-32; C23C014-56; H01L021-20
 ICS C23C014-34; C23F001-02; H01L021-203

AB EP 866146 A UPAB: 19981021

The apparatus comprises a shield for **lining** a portion of the interior of a vacuum processing **chamber**, with the interior of the shield defining a shield passage which contains a heater element. A gas inlet supplies gas to the shield passage.

Also claimed are: (i) a processing **chamber** having a vacuum **chamber** and a shield **lining** as above;
 (ii) a sputtering process; (iii) a **chamber** for processing a rectangular substrate; and (iv) a bake-out **process** for a **semiconductor processing chamber**.

USE - The apparatus is used for processing **semiconductor wafers**, especially those used as one-piece items.

ADVANTAGE - Reduced particulate contamination of workpieces is obtained by effective **temperatur control** of the shield.

Dwg.0/5

FS CPI
FA AB
MC CPI: M13-G02

L165 ANSWER 24 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1995-263245 [34] WPIX

DNN N1995-202378 DNC C1995-119914

TI **Semiconductor processing chamber** - has a double-walled **chamber** having solid metal-gettering material pellets in gap between walls.

DC L03 U11

IN CHIOU, H; TORRES, R P

PA (CHIO-I) CHIOU H; (TOYJ) TOSOH CORP

CYC 1

PI US 5434090 A 19950718 (199534)* 8p C23C016-00

ADT US 5434090 A US 1993-172988 19931227

PRAI US 1993-172988 19931227

IC ICM C23C016-00

AB US 5434090 A UPAB: 19950904

A **chamber** (10) for **processing** a **semiconductor** substrate comprises (a) a first tube (11) with a processing zone contained in at least a portion of the inner surface, (b) a second tube (12) surrounding at least part of the first tube, and (c) a gap (14) between the two tubes, separated by the first tube from the processing zone and filled with a solid metal-gettering material (20).

A processing **chamber** comprising a furnace tube and a rapid thermal processor are claimed.

Also claimed is a **process** for **semiconductor processing**.

The solid gettering material (20) in the gap (14) between the outer surface (1112) of inner tube (11) wall (111) and the inner surface (1201) of outer tube (12) wall (121) is in the form of pellets 0.1 to 3.0 mm selected from undoped or doped polysilicon, carbon, silicon, germanium, silicon carbide and silicon nitride. Purge gas **inlet** and **outlet ports**

extends through the wall (121) into the gap (14) with quartz wool adjacent the **port** to reduce the likelihood of the metal gettering particles leaving the gap (14).

USE - A double walled **chamber** for **processing semiconductor** substrates.

ADVANTAGE - Pellets provide increased metallic gettering efficiency due to the large surface area. Purge gas in gap reduces pellet oxidn.. HCl is eliminated from the gap reducing health and safety concerns and wear and tear on equipment and exhaust systems. Substrates have less sodium concn. than those processed with a conventional single walled furnace tube. The double walled furnace tube with the pellets eliminate the danger of electrocution compared

to a **liner** lying outside a conventional furnace tube and the particulate problems with a line slid inside a furnace tube. A lower thermal mass allows the furnace tube with pellets to ramp down at a higher rate than a furnace tube with **liner** decreasing the process cycle time. The double walled furnace tube with pellets costs less than a conventional single walled tube with **liner**, and would not need replacing if pellets break.

Dwg.3/5

FS CPI EPI
FA AB; GI
MC CPI: L04-C16; L04-D05
EPI: U11-C03A

L165 ANSWER 25 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1995-017133 [03] WPIX

DNN N1995-221945 DNC C1995-132094

TI Vertical heat treatment appts. for **processing** large dia. **semiconductor** wafers, etc. - with rotary holder turning independently of **liner** plate allowing large dia. wafers to be rapidly heated with uniform temp. distribution for high precision treatment.

DC L03 U11 U14

IN OHKASE, W

PA (TKEL) TOKYO ELECTRON LTD; (TKEL) TOKYO ELECTRON SAGAMI LTD; (TKEL) TOKYO ELECTRON TOHOKU KK

CYC 2

PI JP 06302523 A 19941028 (199503)* 8p H01L021-205

US 5443648 A 19950822 (199539)B 10p C23C016-00

JP 3190165 B2 20010723 (200143) 9p H01L021-205

ADT JP 06302523 A JP 1993-86340 19930413; US 5443648 A US 1994-225618 19940411; JP 3190165 B2 JP 1993-86340 19930413

FDT JP 3190165 B2 Previous Publ. JP 06302523

PRAI JP 1993-86340 19930413

IC ICM C23C016-00; H01L021-205

ICS H01L021-31; H01L021-324

AB US 5443648 A UPAB: 19951004 ABEQ treated as Basic

A vertical heat treatment appts. comprises a vertical processing **vessel** (11) including a heat source (21,22,23), and a loading mechanism (31) for holding an object to be treated and loading into the **vessel** from below. The loading mechanism includes a lift member (33) to be loaded and unloaded through the bottom by a lift drive unit (32). A **liner** plate (34) is present on the lift member and a rotary holder (35) holds the object to be treated (W) horizontally above the plate while turning it independently of the plate. The rotary holder can be moved up-and-down between object heating positions and treating positions independently of the **liner** plate.

Also claimed is an appts. as above additionally comprising a loading **chamber** below the processing **vessel**, and a furnace **port** shutter and partition shutter which are hollow discs through which water can pass and which close the furnace **port** and partition the loading **chamber**

when the atmos. is to be replaced with inert gas.

USE - Used for **processing** large dia.

semiconductor wafers and LCD substrates and as oxidn. and CVD appts..

ADVANTAGE - Rapid, even heating of large wafers, etc. is achieved, temp. distribution is uniform and precise heat treatment is possible.

Dwg.1/4

AB JP 06302523 A UPAB: 20010801

Dwg.1/4

FS CPI EPI

FA AB; GI

MC CPI: L04-D05

EPI: U11-C03A; U11-C05B1; U11-C09B; U14-K01A

L165 ANSWER 26 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1995-005716 [01] WPIX

DNN N1995-004778 DNC C1995-001839

TI **Ceramic** electrically insulative **liner** - protects conductive surfaces in a plasma processing **reactor**.

DC L02 L03 M13 P78 U11 V05 X14

IN LAW, K S; ROBERTSON, R; WHITE, J M

PA (MATE-N) APPLIED MATERIALS INC

CYC 2

PI US 5366585 A 19941122 (199501)* 11p B44C001-22

JP 06298596 A 19941025 (199502) 9p C30B025-08

ADT US 5366585 A US 1993-10975 19930128; JP 06298596 A JP 1994-8690 19940128

PRAI US 1993-10975 19930128

IC ICM B44C001-22; C30B025-08

ICS B01J019-08; H01L021-302

ICA H01L021-31

AB US 5366585 A UPAB: 19950110

A processing **chamber** (200) is improved using a free-standing electrically insulative **liner** (220-223). A processing plasma is generated in plasma processing region (214) adjacent to a substrate (215) held on a substrate holder (216).

Liner (220-223) is disposed adjacent to the metallic walls (212) of process **chamber** (200) facing the plasma. Also claimed is a processing system (200) comprising vacuum **chamber** (213) having electrically conductive walls; plasma generator electrode (216) within vacuum **chamber** (213) adjacent to substrate (215) being processed, gas **ports** to the **chamber** (213) provides a gas for the plasma.

Electrically insulative **liner** (220-223) covers portions of walls (212) facing the plasma. The **liners** have an effective plasma electrical barrier thickness substantially greater than 200 Angstroms. Also claimed is a method of protecting conductive portions of a plasma processing **chamber** (200) which involves providing the insulative **liner** (220-223) in processing **chamber** (200).

USE - **Ceramic** electrically insulative **liner**

is used to protect conductive, typically metallic surfaces of a process **chamber** which can potentially be contaminated during plasma processing e.g. it can be used in a substrate processing **reactor chamber**; chemical vapour deposition CVD or plasma enhanced CVD processing **reactor chambers**.

ADVANTAGE - The **liner** reduces the deposit of cpds. formed from the plasma on protected reaction **chamber** surfaces, and thus avoids the formation of a source of particulates. The **liner** enables cleaning of the **reactor chamber** walls using an etch plasma generated from a halogen-comprising gas without the etch plasma attacking protected metallic portions of the **reactor**. The **reactor** walls can be etch cleaned in a manner which does not cause a gradual build up of contaminants on the walls. The **liner** can serve additional function of preventing arcing or local intense plasma discharged from a plasma generating electrode, to a conductive portion of the **reactor chamber**.

Dwg.2A/2

FS CPI EPI GMPI

FA AB; GI

MC CPI: L04-C01B; M13-E07

EPI: U11-C09B; U11-C09C; V05-F05C; V05-F08D1; X14-F02

L165 ANSWER 27 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1994-302093 [37] WPIX

CR 1993-413367 [51]

DNC C1994-137737

TI Apparatus for elimination of contaminant formation - in the CVD of titanium nitride from titanium chloride and ammonia..

DC L02 L03 M13

IN CHURLEY, M J; EICHMAN, E C; RAMSEY, W C; SOMMER, B A

PA (MATE-N) MATERIALS RES CORP

CYC 1

PI US 5348587 A 19940920 (199437)* 6p C23C016-50

ADT US 5348587 A Cont of US 1992-976516 19921116, US 1993-133582 19931007

FDT US 5348587 A Cont of US 5271963

PRAI US 1992-976516 19921116; US 1993-133582 19931007

IC ICM C23C016-50

AB US 5348587 A UPAB: 19941109

Apparatus for **processing semiconductor**

wafers comprising; a) CVD reaction **chamber**

bounded by a sealable cold wall and a wafer supporting susceptor and a heater to heat the wafer to a primary reaction temperature, reaction gas **inlet** and **outlet**, positioned such that reaction gases from the **inlet** flow against the susceptor and downstream to the **outlet**. b) Surface **liner** on the cold wall partially thermally insulated from it and downstream from the susceptor. c) Secondary electrode downstream of the susceptor. d) Electrical potential source connected to the secondary electrode sufficient to form a low energy plasma in gas

between the secondary electrode and at least a portion of the **reactor** surfaces that are in contact with gases flowing downstream of the susceptor to raise their temperature to avoid formation of undesirable contaminants but below the primary reaction temperature.

USE - Cold wall **CVD reactors** for titanium nitride deposition.

ADVANTAGE - Downtime of the **reactor** is reduced by reducing contamination.

Dwg.1/1

FS CPI
FA AB; GI
MC CPI: L04-C12B; L04-D01; M13-E02; M13-E06; M13-E07
DRN 1686-S; 1686-U; 1713-S; 1713-U

L165 ANSWER 28 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1994-279251 [34] WPIX

DNC C1994-127399

TI Consolidating and eliminating voids from unidirectional, continuous, fibre-reinforced polymeric prepreg - by heating it, pulling it over and under stationary bars to flatten it and reshaping it by passing it through matched grooves between a pair of loaded, cooled nip rollers.

DC A32

IN SANDUSKY, D A

PA (USAS) NASA US NAT AERO & SPACE ADMIN

CYC 1

PI US 141292 A0 19940815 (199434)* 21p B29C000-00

US 5395477 A 19950307 (199515) 10p B29B011-16

ADT US 141292 A0 US 1993-141292 19931020; US 5395477 A US 1993-141292 19931020

PRAI US 1993-141292 19931020

IC ICM B29B011-16; B29C000-00

ICS B29B015-14; B29K105-08

AB US N8141292 N UPAB: 20011211

Uniform, consolidated prepreg tow is prepd. by (i) heating unconsolidated, unidirectional, continuous, filament-reinforced polymeric material (102) to cause the polymer to change from solid to viscous liq., (ii) passing the material continuously over one stationary bar and under a second so that pressure gradients are imposed on it to consolidate and flatten it, and (iii) reshaping the malleable, consolidated, flattened prepreg by passing it through a shaped, matched groove between loaded, cooled nip rollers (104).

USE - Method and appts. are used to prepare prepreg ribbons and tapes which are free of voids.

ADVANTAGE - Method and appts. do not require use of a pultrusion die and fibre balls and dry filament areas on the unconsolidated prepreg can pass through the appts. freely instead of causing breakages because there is no rigid **die** entry.

Processing rates for slurry powder coated thermoplastics can be as high as 50 feet per minute.

Dwg.1a/5

ABEQ US 5395477 A UPAB: 19950425

Appts. for consolidating a pre-impregnated, filament-reinforced polymeric prepreg material, comprises:

(a) a supply means for delivering a pre-impregnated, filament-reinforced polymeric prepreg material;

(b) a forming means, spaced in an operable relationship to the supply means, for expelling voids and pre-shaping the pre-impregnated, filament-reinforced polymeric prepreg material into a malleable, wide, flat cross-sectional form, where the forming means comprises a tube furnace, a **steel tube liner** having an entry side and an exit side disposed within the tube furnace, a pre-melting **chamber** disposed within the **steel tube liner** near the entry side, and a stationary bar assembly disposed within the **steel tube liner** near the exit side;

(c) a shaping means, spaced in an operable relationship to the forming means, for re-shaping the malleable, wide, flat pre-impregnated filament-reinforced polymeric prepreg material into a solid, shaped, consolidated, filament-reinforced polymeric material, where the shaping means is a loaded, convection cooled, nip-roller apparatus comprising two hollow, matched, grooved rollers forming a nip point where one of the rollers is loaded against a fixed roller; and

(d) a take-up means for pulling the pre-impregnated, filament-reinforced polymeric prepreg material from the supply means, through the forming means and the shaping means, and taking up the solid, shaped, consolidated, filament-reinforced polymeric material.

The stationary bar assembly comprises a bar fixture supporting a plurality of bar templates which further support pair(s) of stationary bars, where the bars are oriented perpendicularly to the pre-impregnated filament-reinforced polymeric material in its axial direction.

USE/ADVANTAGE - For prepreg ribbons, tapes, etc.. Superior quality and consistency.

Dwg.0/5

FS

CPI

FA

AB; GI

MC

CPI: A11-A02; A11-B09C; A11-C04; A12-S08

PLC

UPA 20011211

KS: 0011 0016 0020 0031 0229 1285 2212 2215 2220 2368 2371 2413 2491
2505 2506 2510 2532 2542 2560 2815 3240 3241

FG: *001* 017 03- 141 151 27- 308 309 369 387 393 395 397 398 428
437 439 46& 479 487 512 53& 54& 602 654 668 684 722 723

PLE

UPA 20011211

[1.1] 017; P1081-R F72 D01; S9999 S1514 S1456; S9999 S1650
S1649; H0317; S9999 S1387; S9999 S1058 S1014; S9999
S1605-R

[1.2] 017; ND07; N9999 N6042-R; N9999 N6177-R; K9892; K9789;
N9999 N5812-R; N9999 N6939-R; N9999 N5856; B9999 B3612
B3554

[1.3] 017; A999 A419; S9999 S1149 S1070

L165 ANSWER 29 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1993-158238 [19] WPIX

DNC C1993-070110

TI Prodn. of carbon blanks for electrode mfr., etc. - using press comprising movable **container** with plate between two **chambers**, **nozzle** parts moved by power cylinders, fore **chamber** and loading openings, crosspieces and guide elements.

DC E36 L02 M24 M28

IN KATOSHIN, V N; USTINOV, YU V; VASILIEV, G A

PA (ELEC-R) ELECTRODE IND RES INST

CYC 1

PI SU 1736922 A1 19920530 (199319)* 10p C01B031-02

ADT SU 1736922 A1 SU 1990-4785381 19900122

PRAI SU 1990-4785381 19900122

IC ICM C01B031-02

AB SU 1736922 A UPAB: 19931113

Process includes mixing carbon filler and binder at temp. higher than the softening temp. of binder, cooling to temp. not lower than the softening temp., loading into **container** of **nozzle** press, pre-pressing, pressing of **blank** and thermal **treatment**. An additional product is made by reverse motion of pressing device in a direct opposite to the main extrusion direction. Loading of material for additional prod. prodn. is carried out at the time of pressing the main product, and vice versa. When forming blanks in both directions from material of the same granulometric composition, it is loaded from one common zone. When pressing articles from material of different granulometric compsn., each material is loaded separately.

Press contains movable **container** (1) with press plate (2) separating it into two **chambers** (3) and (4) in which **nozzles** (5) and (6) are located and are moved to the left and right by power cylinders (7) and (8). Loading openings (9) and (10) in **chambers** (3) and (4) are in turn covered by plate (11). Forechamber (12) is located at the centre of plate (11) for loading the material into **container** (1). Left (13) and right (14) crosspieces are mounted on base (15) having guide elements (16), e.g. rollers.

USE/ADVANTAGE - In the production of carbon articles, e.g. sintered and graphite electrodes, blocks for **lining** electrolyzers and **steel**-smelting furnaces, etc. Increased productivity is obtd. Bul.20/30.5.92

Dwg. 1/5

FS CPI

FA AB; GI; DCN

MC CPI: E31-N03; L02-H04; L03-A02B; M24-C; M24-C09

DRN 1669-P

CMC UPB 19931129

M3 *01* C106 C810 M411 M424 M720 M903 M904 M910 N515 Q411 Q453 Q454 Q469

DCN: R01669-P

L165 ANSWER 30 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1993-125665 [15] WPIX

DNN N1993-095915 DNC C1993-055891

TI Die caster and automated casting system - comprises insulated **liner** with shot tube that injects molten metal into die using piston.

DC M22 P53

IN CAUGHERTY, B

PA (CAUG-I) CAUGHERTY B

CYC 1

PI US 5197529 A 19930330 (199315)* 6p B22D017-02

ADT US 5197529 A US 1989-415572 19891002

PRAI US 1989-415572 19891002

IC ICM B22D017-02

ICS B22D017-12

AB US 5197529 A UPAB: 19930924

A die caster comprises a housing (14) **lined** with layers of insulation materials (16) and holding a refractory **liner** (18) that forms a tank for molten metal (28). The metal is poured into the tank through a lid (20). The lid is then closed and heated using heater wires (32) to keep the metal molten. This heating is further assisted by other heater wires (32) that are fitted below the base of the **liner**. The **liner** also has a fused silica short tube assembly (38, 40, 42) embedded in it. This assembly has a piston (56) at one end and a **nozzle** (54) at the housing outlet. Molten metal is ported from the tank (28) and into the first section (38) of the short tube assembly and the piston (56) is then stroked downwards using a hydraulic or pneumatic actuator (62). This forces molten metal out of the **nozzle** and injects it, under pressure, into the die (12).

Also claimed is the die caster used with a die (12) that has ejector pins to eject the die casting after it has solidified.

USE/ADVANTAGE - To provide a die caster that allows Al alloy castings to be produced in an automated hot **chamber die casting process**.

1/5

FS CPI GMPI

FA AB; GI

L165 ANSWER 31 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1992-218826 [27] WPIX

DNN N1992-166163 DNC C1992-099048

TI **Semiconductor processing** module for placement in reaction **chamber** - having heat transmitting multilayered window with purge gas passages.

DC L03 M13 U11

IN MOSLEHI, M M

PA (TEXI) TEXAS INSTR INC

CYC 7

PI EP 492632 A1 19920701 (199227)* EN 17p C23C016-48

R: DE FR GB IT NL

JP 04294526 A 19921019 (199248) 14p H01L021-205
 US 5275976 A 19940104 (199402) 13p H01L021-00
 EP 492632 B1 19950412 (199519) EN 18p C23C016-48

R: DE FR GB IT NL

US 5405444 A 19950411 (199520) 13p C23C016-00
 DE 69108876 E 19950518 (199525) C23C016-48

ADT EP 492632 A1 EP 1991-122256 19911227; JP 04294526 A JP 1991-347002
 19911227; US 5275976 A US 1990-634676 19901227; EP 492632 B1 EP
 1991-122256 19911227; US 5405444 A Div ex US 1990-634676 19901227,
 US 1993-151082 19931112; DE 69108876 E DE 1991-608876 19911227, EP
 1991-122256 19911227

FDT US 5405444 A Div ex US 5275976; DE 69108876 E Based on EP 492632

PRAI US 1990-634676 19901227

REP EP 255454; EP 299247

IC ICM C23C016-48; H01L021-205

ICS C30B031-12; H01L021-02; H01L021-302; H01L021-31; H01L021-324;
 H01L021-463

AB EP 492632 A UPAB: 19931006

Semiconductor wafer (18) is supported in a reaction **chamber** (16) in a module (56) with its back surface facing a stack of heat transmitting windows (100,110). The windows are provided with channels, which allow a purge gas to flow from one window to the next, and spacers between the windows so that a portion of the gas can move radially and axially within the gap. The module has **inlet** and **outlet ports** to receive the gas at the **inlet** and to pass at least a portion of the gas via the **outlet** into the process **chamber** (16).

USE/ADVANTAGE - In the deposition of material onto the face of semiconductor wafers to form e.g. epitaxial, dielectric, metal, polycrystalline silicon, and doping oxide layers. Window, which conducts heat radiation through to the back of the semiconductor wafer, can be heated by radiation of thermal energy from the wafer, which can cause deposition of material onto the window, as well as on the face of the wafer, reducing its transmissivity to the radiation from the lamp used to heat the wafer, which causes further heating of the window and deposition of material on the window, degrading the processing and causing particle generation in the process **chamber**. Cooling the window by purge gases prevents deposition on the window while purge gas flow prevents deposition on the back of the wafer; simplifying the fabrication process.

3/11

ABEQ US 5275976 A UPAB: 19940223

Purging from a side of a **semiconductor wafer**, reactive **process** gases comprises (a) placing layered stack of windows, each openable to pass heat energy through, in a process **chamber**; (b) flowing purge gas through channels in the windows from one to the next adjacent window; (c) maintaining a gap between the windows and permitting part of the gas to move radially and axially within the gap.; and (d) receiving purge gas at **inlet** part of layered stack, passing at least part of purge

gas received through an **outlet** in the windows.

USE/ADVANTAGE - As a process **chamber** purge module, used for **semiconductor processing** appts. Maintains **chamber** cleanliness in **semiconductor processing reactors**.

Dwg.0/11

ABEQ EP 492632 B UPAB: 19950524

A module for placement within a semiconductor for device fabrication **reactor** process **chamber** provided with an optical/quartz window, said module being positioned on the backside of a semiconductor wafer onto which there is to be deposited material as a result of reactive gases surrounding said semiconductor wafer, comprising: a layered stack of windows and operable for passing heat energy therethrough; channels for allowing a purge gas to flow from one window to the window in the next adjacent layer; spacers for maintaining a gap between said window layers so that a portion of said gas can move radially and axially within said gap; **inlet** and **outlet ports** within said module so as to receive said purge gas at said **inlet** and to pass at least a portion of said received purge gas via said **outlet** into said process **chamber**, said module being positioned between the optical/vacuum quartz window and the semiconductor wafer.

Dwg.2/11

ABEQ US 5405444 A UPAB: 19950530

A module for placement within a semiconductor device fabrication **reactor** process **chamber** comprises (a) a layered stack of windows operable for passing heat energy, (b) channels to allow a purge gas to flow from one window to the window in the adjacent layer (c), spacers to maintain a gap between the window layers so that a portion of the gas can move radially and axially within the gap, and (d) **inlet** and **outlet ports** within the module to receive the purge gas to the **inlet** and to pass at least a portion of the received purge gas via the **outlet** to the process **chamber**. A process **chamber liner** isolates the semiconductor **wafer** from the process **chamber** walls, to reduce cross contamination between the wafer and **chamber** wall.

USE/ADVANTAGE - Used for depositing films on semiconductor wafers. Minimised equipment-induced contamination of wafers.

Dwg.3/11

FS CPI EPI

FA AB; GI

MC CPI: L04-D01; L04-D10; M13-E01; M13-E07
EPI: U11-C09A; U11-C09C

L165 ANSWER 32 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1991-216590 [30] WPIX

DNC C1991-094007

TI Coating inner surface of annular components with diamond - by chemical vapour deposition from

hydrocarbon-hydrogen mixt. used for coating valves and spray
nozzles, etc..

DC L02 M13

IN BANHOLZER, W F; JOHNSON, R N; LEONARD, G L; MEHAN, R L; SPIRO, C L

PA (GENE) GENERAL ELECTRIC CO

CYC 13

PI EP 437830 A 19910724 (199130)*

R: AT BE CH DE FR GB LI SE

CA 2031098 A 19910717 (199139)

ZA 9100021 A 19920129 (199209)

JP 04214869 A 19920805 (199238)

EP 437830 B1 19941214 (199503) EN 5p C23C016-26

R: AT BE CH DE FR GB LI SE

DE 69015146 E 19950126 (199509) C23C016-26

IE 66256 B 19951227 (199609) C23C016-26

US 5508071 A 19960416 (199621) 4p B05D003-00

ADT EP 437830 A EP 1990-125424 19901224; ZA 9100021 A ZA 1991-21
19910102; JP 04214869 A JP 1991-15945 19910114; EP 437830 B1 EP
1990-125424 19901224; DE 69015146 E DE 1990-615146 19901224, EP
1990-125424 19901224; IE 66256 B IE 1991-119 19910115; US 5508071 A
Div ex US 1990-464818 19900116, US 1993-127964 19930928

FDT DE 69015146 E Based on EP 437830

PRAI US 1990-464818 19900116; US 1993-127964 19930928

REP 2.Jnl.Ref; JP 01059071; JP 63026371; JP 63315597; US 4483892;
03Jnl.Ref; EP 421276

IC ICM B05D003-00; C23C016-26

ICS C30B029-04

AB EP 437830 A UPAB: 19930928

An annulus is placed in a reaction **vessel** and heated in a
temp at which diamond is **deposited** by **chemical**
vapour deposition. A gaseous hydrocarbon-hydrogen
mixture supplied to the **chamber** is at least partially
decomposed therein and directed onto the inner surface of the
annulus to deposit a layer of diamond.

The hydrocarbon is pref methane, and the molar ratio of
hydrocarbon:hydrogen is 1:10 to 1:1000, the mixture may additionally
contain an inert gas. Pressure in the **chamber** is
0.01-1000, esp. 100-800 torr, and deposition temp 500-1100 deg C,
esp 850-950 deg C. Decompsn may be affected by contact with a W, Mo
or Ta filament maintained at 1500-2800 deg. C andm the deposited
diamond layer may have a thickness of 1-50 microns.

There is claimed independently an annulus the inner surface of
which is coated with diamond formed by **chemical**
vapour deposition, the diamond being under
compressive stress.

USE- Deposition on metal, alloy, ceramic, glass or carbon (all
claimed). Partic wire drawing dies, spray **nozzles**, valves,
injectors, extrusion sadie **liners**, mould **liners**
and injection **liners**. @ (4pp Dwg.No. 0/0) temp

ABEQ EP 437830 B UPAB: 19950126

A flow control component having n annulus which includes not only
full 360 deg. annuli of cylindrical or other configuration but also

includes partial annuli so long as a sufficient concave surface is presented for exerting compression on the deposited CVD diamond layer, the interior surface of the annulus being at least partially coated with a layer of diamond applied by a **chemical vapour deposition** process.

Dwg.0/0

ABEQ US 5508071 A UPAB: 19960529

A method for improving the abrasion resistance of the annular interior surface of an annulus having an exterior surface, comprises: (a) placing the annulus in a **chamber** and heating to an elevated CVD diamond-forming temp.; (b) providing a hydrogen/hydrogen gaseous mixt. within the **chamber**; (c) at least partially decomposing the gaseous mixt. in the **chamber** to form a CVD diamond layer on the entire interior and exterior surface of the annulus; and (d) quenching the annulus by rapidly reducing the temp. of the annulus for removing the CVD diamond layer from the exterior surface of the annulus by spalling while retaining the CVD diamond layer on the interior surface of the annulus. The annulus is formed of a material having a higher coefft. of thermal expansion than diamond sufficient for enhancing retention of diamond within the annular interior surface due to compressive forces and removal of diamond on the exterior surface during the quenching due to spalling.

Dwg.0/0

FS CPI

FA AB

MC CPI: L02-A; L02-F05; L02-H04; M13-E02

L165 ANSWER 33 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1991-028986 [04] WPIX

DNN N1991-022339 DNC C1991-012422

TI **CVD reactor** for silicon prodn. - includes removable **liner** box having non-contaminating deposition surface.

DC J04 L03 U11 U12 X15

IN DANIELS, G A; GAUTREAU, M F; HUGHMARK, G A; LAWRENCE, W W

PA (ETHY) ETHYL CORP

CYC 1

PI US 4981102 A 19910101 (199104)*

ADT US 4981102 A US 1986-833256 19860227

PRAI US 1984-599350 19840412; US 1986-833256 19860227

IC C23C016-24

AB US 4981102 A UPAB: 19930928

CVD reactor for growing high purity Si comprises an insulated housing contg. a removeable **liner** box having a non-contaminating deposition surface which defines a gas flow-path. Also included is a turbulent gas flow supply, exhaust and **temp. control**. The deposition surface is pref.

made of Mo, graphite, Si₃N₄, SiC, Si, quartz or SiON.

USE/ADVANTAGE - In prodn. of high purity semiconductor poly Si for solar cell etc. mfr. **Reactor** provides very high

deposition rates at low cost and with min. heat losses.
3/4

FS CPI EPI
FA AB; GI
MC CPI: J04-X; L04-A01; L04-D01
EPI: U11-C01B; U11-C01J2; U11-C09B; U12-A02A3; X15-A02A
DRN 1247-U; 1666-U; 1694-U; 1778-U

L165 ANSWER 34 OF 42 WPIX (C) 2002 THOMSON DERWENT
AN 1991-026986 [04] WPIX
DNN N1991-020703 DNC C1991-011723
TI Preventing staining and corrosion of aluminium vacuum
chamber - by **lining** inner wall with aluminium
foil.

DC L03 M13 U11
PA (SHOA) SHOWA ALUMINIUM CO LTD
CYC 1

PI JP 02298335 A 19901210 (199104)*
ADT JP 02298335 A JP 1989-119970 19890512
PRAI JP 1989-119970 19890512
IC B01J003-00; C23C016-44; C23F004-00; H01L021-20
AB JP 02298335 A UPAB: 19930928

Staining and corrosion are prevented by **lining** the inside
wall of the vacuum **chamber** with aluminium foil.

USE/ADVANTAGE - Staining and corrosion of an Al vacuum
chamber used for MBE, ion plating, dry etching, or
CVD apparatus are effectively prevented.

In an example, a soln. contg. 60 wt.% of SiO₂ ceramic powders
of 1 micron dia. dispersed in isopropylalcohol was coated on one
face of aluminium foil, and the coating was dried and baked at 150
deg.C to form a 15 microns thick ceramic coating. The foil was
lined on the inside wall of an aluminium vacuum
chamber. Reactive ion beam etching was carried out using
CCl₄ at a 10 power -4 Torr in the **lined** vacuum
chamber. The foil was replaced each time. No corrosion was
observed on the inside wall of the vacuum **chamber**.

0/0

FS CPI EPI
FA AB
MC CPI: L04-D01; M13-E07
EPI: U11-C09B; U11-C09C; U11-C09X

L165 ANSWER 35 OF 42 WPIX (C) 2002 THOMSON DERWENT
AN 1989-125372 [17] WPIX
DNN N1989-095439 DNC C1989-055537
TI Engine cylinder head heat insulation - thin ceramic plate defining
space filled with heat insulating material.

DC L02 M13 Q52
PA (ISUZ) ISUZU MOTORS LTD
CYC 1

PI JP 01069758 A 19890315 (198917)* 7p
JP 2540878 B2 19961009 (199645) 5p F02F001-24

ADT JP 01069758 A JP 1987-223977 19870909; JP 2540878 B2 JP 1987-223977 19870909

FDT JP 2540878 B2 Previous Publ. JP 01069758

PRAI JP 1987-223977 19870909

IC C23C016-30; F02F001-24

ICM F02F001-24

ICS C23C016-30; C23C016-32

AB JP 01069758 A UPAB: 19930923

Ceramic head liner body is composed of ceramic thin plate at the side of the combustion **chamber** of the **liner** body through a heat insulation material. The cementing portions of the head **liner** body, the heat insulation material and the thin plate is coated with ceramic material by **CVD**. The heat insulation material is sealed in a space formed with the head **liner** body and the thin plate.

The head **liner** body and the thin plate is pref., constituted by Si-nitride. The heat insulation material is a fired mixt. of Si-nitride fibre and alumina fibre or K-titanate fibre.

USE/ADVANTAGE - For ceramic engines, minimizing thermal energy dissipating to outside through the cylinder heads and cylinder blocks.

0/5

FS CPI GMPI

FA AB

MC CPI: L02-D15; L02-J02C; M13-E02

L165 ANSWER 36 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1988-271712 [39] WPIX

DNN N1988-206349 DNC C1988-120945

TI **Reactor** for epitaxial deposition of semiconductor - is integrated with wafer transfer to and from carrier e.g. cassette, giving reduced particle-contamination.

DC L03 P62 Q35 U11

IN DAN, J P; DEBONI, E; FREY, P; IFANGER, J; DAN, J; DE, BONI E

PA (SITE-N) SITESA SA

CYC 15

PI DE 3707672 A 19880922 (198839)* 19p

WO 8807096 A 19880922 (198840) EN

RW: BE CH DE FR GB IT LU NL SE

W: JP US

EP 285840 A 19881012 (198841) DE

R: AT BE CH DE ES FR GB GR IT LI LU NL SE

EP 305461 A 19890308 (198910) DE

R: AT BE CH DE ES FR GB GR IT LI LU NL SE

DE 3744846 A 19890803 (198932)

JP 01502512 W 19890831 (198941)

US 5038711 A 19910813 (199135)

EP 305461 B1 19930107 (199302) DE 28p C30B025-02

R: AT BE CH DE ES FR GB GR IT LI LU NL SE

DE 3877288 G 19930218 (199308) C30B025-02

ADT DE 3707672 A DE 1987-3707672 19870310; WO 8807096 A WO 1988-EP188 19880310; EP 285840 A EP 1988-103800 19880310; EP 305461 A EP

1988-902452 19880310; DE 3744846 A DE 1987-3744846 19870310; JP 01502512 W JP 1988-502423 19880310; US 5038711 A US 1989-274805 19890105; EP 305461 B1 EP 1988-902452 19880310, WO 1988-EP188 19880310; DE 3877288 G DE 1988-3877288 19880310, EP 1988-902452 19880310, WO 1988-EP188 19880310

FDT EP 305461 B1 Based on WO 8807096; DE 3877288 G Based on EP 305461, Based on WO 8807096

PRAI DE 1987-3707672 19870310; DE 1987-3744846 19870310

REP 2.Jnl.Ref; A3...8851; DE 3204436; EP 147967; EP 85397; No-SR.Pub; US 4322592; US 4632060; US 4638762

IC ICM C30B025-02

ICS B25J009-00; B65G047-06; B65G049-06; C23C016-00; C30B025-12; C30B025-14; C30B025-16; C30B031-06; C30B035-00; G01J005-00; H01L021-20; H05B006-02

AB DE 3707672 A UPAB: 19930923

The **reactor** construction and esp. the gas flow provisions reduce the contact between particles, contd. in the **reactor** gas or generated in the **process** and the **wafers** (70) as well as the susceptor (50). The **reactor** consists of a **chamber** (10) contg. the susceptor (50), pref. made of graphite, a gas-**inlet** diffusor (120) and an **outlet** (13). A gas-mixer is also provided outside the **chamber**. The susceptor is pref. heated by induction using HF-power from a generator (510) conducted in a spiral surrounding the **chamber** and incorporating cooling and reflector (512). The HF frequency range is 15-100 KHz, pref. 16-25 KHz. A pyrometer (400) detects and evaluates the radiation, pref. at 2 wavelengths, of the susceptor through windows between spiral windings and is used to **control** the **temp.** and decode the susceptor code, consisting of a combination of thick and thin areas of the susceptor wall, via a controller (500). The susceptor can be moved from the **chamber** vertically into the load/unload position, which is contd. inside the same clean air ambient. A laminar air or gas flow is maintained over the susceptor via the **gas-inlet** from the **reactor**.

USE/ADVANTAGE - The laminar flow ensures reduced incidence of particle deposition from the gas on the wafers. Due to the use of a single cabinet for loading, deposition and unloading a clean air ambient can be more easily maintained. The design of the **reactor** also minimises particle generation.

1/9

ABEQ EP 305461 B UPAB: 19930923

Epitaxial facility for the application of semiconducting layers onto semiconductor wafers (70), with at least one reaction **chamber** (10) to accommodate a rotatable support (50) shaped as a truncated pyramid for holding the wafers, the **chamber** being provided with at least one gas **inlet** and one gas **outlet** for the admission and discharge of supporting, reaction and scavenging gases, as well as pure air and/or a protective gas, where a gas mixing device (100) for mixing the gases is provided upstream of the gas **inlet**, characterised in that the epitaxial facility comprises a pair of reaction

chambers (10, 10') which are set up identically as far as connections, flows, and operating techniques are concerned, the two **chambers** being arranged so their wafer support (50) can be loaded independently, and that the epitaxial processes in them can be performed independently, where the gas mixing device (100) comprises a main gas line (101) hooked up to the gas **inlets** of the reaction **chambers** (10, 10') through symmetric junctions, and several branch lines (102-107, 110) opening sequentially into successive points of the main line (101) for the in-feed of reaction and scavenging gases, these gases being fed, during the junctioning of the facility, according to their technical purity and corrosiveness into branch lines which succeed each other register-fashion in such a way that the less pure and more aggressive gases are fed preferentially into the branch lines located closest to the gas **outlet** (108, 109) of the gas mixer (100), and that at least the two branch lines (107, 110) which enter most downstream into the main line are each connected to the latter through a pair of ducts which enter it symmetrically.

1/9

ABEQ US 5038711 A UPAB: 19930923

Appts. for depositing an epitaxial layer on multiple semiconductor wafers comprises an elongate **chamber** (16) with gas **inlet** and **outlet** in opposite end walls for flow parallel to the longitudinal axis. A wafer support with axis of symmetry parallel to the gas flow direction has a polygonal cross-section with rounded corners.

The support is formed as a truncated pyramid (50) with base tapering outwardly towards the **outlet** end, and a second truncated pyramid (56) of the same shape and size with its base adjacent to the first pyramid base. A cap (55) on the support end adjacent to the gas **inlet** is shaped to promote laminar flow along the support. A **lining** (210) is connected to the **outlet** end wall receives and retains part of the contaminants in the gas flow.

ADVANTAGE - Increases evenness and purity of the epitaxial layer by minimising contact of wafers with undesirable microscopic particles.

1

FS CPI EPI GMPI

FA AB; GI

MC CPI: L04-C01

EPI: U11-C01B; U11-C01J1; U11-C09B; U11-F02A1

L165 ANSWER 37 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1988-113691 [17] WPIX

DNN N1988-086409 DNC C1988-050882

TI Rocket propulsion system for aircraft - **has** combustion **chamber** surrounded by hollow double wall **of** silicon carbide fibre cloth, as fuel duct where fuel is **pyrolysed**.

DC H06 K04 L02 Q25 Q53 Q73

IN COFFINBERR, G A

PA (GENE) GENERAL ELECTRIC CO

CYC 5

PI DE 3734100 A 19880421 (198817)* 13p

GB 2196393 A 19880427 (198817)

FR 2610044 A 19880729 (198837)

US 4840025 A 19890620 (198931) 11p

CN 87106915 A 19881130 (198946)

GB 2196393 B 19910717 (199130)

ADT DE 3734100 A DE 1987-3734100 19871009; GB 2196393 A GB 1987-24106
 19871014; FR 2610044 A FR 1987-13895 19871008; US 4840025 A US
 1988-183471 19880415

PRAI US 1986-918214 19861014; US 1988-183471 19880415

IC B64D027-02; B64D037-34; C06D005-00; C06D006-60; C10G047-02;
 F02K007-10; F02K009-62; F23R003-44

AB DE 3734100 A UPAB: 19930923

Propulsion system, with (i) a rocket case, contg. a combustion chamber, fuel injection devices, a throat and a nozzle, (ii) a fuel duct, in which fuel is endothermically pyrolysed, and which directly surrounds the combustion chamber and throat, and (iii) a device for producing a fuel flow in the duct, is characterised in that the fuel duct has (a) an internal wall of SiC fibre fabric, which forms a lining for the combustion chamber and throat, the SiC fibres being woven so that heat is conducted from the combustion chamber and throat so as to provide heat for the endothermic pyrolysis of the fuel passing through the duct, and (b) an external wall of SiC fibre fabric.

USE/ADVANTAGE - The system can be used in aircraft with propulsion by rocket, ram jet or ram jet with supersonic combustion. The overall design permits a twin fuel system, including liq. H₂, to be accommodated without vacuum tanks, coolants or other bulky devices for thermal insulation. The endothermic pyrolysis (a) helps to cool the walls of the combustion chamber and throat, and (b) produces from a fuel mixt. contg. H₂ and a hydrocarbon, e.g. C₂H₄, a mixt., now contg. e.g. C₂H₂, which has higher combustion rate and/or higher combustion temp. and/or lower mol.wt.

0/6

ABEQ GB 2196393 B UPAB: 19930923

In a propulsion system having a rocket engine including a combustor, propellant injectors, nozzle throat and nozzle; a fuel passageway adjacent to and surrounding the combustor and nozzle throat; and means providing for fuel flow in the fuel passageway; the inclusion of a woven silicon carbide fiber inner wall forming a combustor liner and a nozzle throat liner and a woven silicone carbide fiber outer wall spaced from the inner wall to form said fuel passageway, the silicon carbide fibers being so woven as to conduct heat from the combustor and nozzle throat to the fuel passageway, thereby to provide heat for the endothermic pyrolysis of the fuel in said passageway.

ABEQ US 4840025 A UPAB: 19930923

A rocket propulsion system has a casing containing a combustor,

propellant injectors, **nozzle** throat and **n zle**, and a passageway in which fuel is endothermically pyrolysed and which is adjacent to and surrounds the combustor and throat. A woven silicon carbide fibre inner wall forms a **combustor** and throat **liner**, and a similar outer wall is spaced from the inner to form the passageway.

The fibres are woven to conduct heat from the combustor and throat to the passageway, providing heat for pyrolysis. The fibres are pref. wound circumferentially to provide high-pressure containment for combustor and throat, and are treated by **chemical vapour deposition** or infiltration of an organometallic cpd. to provide a porosity for selectively controlling hydrogen diffusion through the woven material.

USE/ADVANTAGE - Partic. for rocket, **scram jet** or ram **jet** engines, improves the cooling of combustor and throat **liners**.

FS CPI GMPI

FA AB

MC CPI: H06-B03; K04-C01; L02-E05; L02-H02A

DRN 0326-U; 0327-U; 1247-U

L165 ANSWER 38 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1985-032627 [06] WPIX

DNN N1985-024219

TI V-engine with pressure-cast block - has longitudinal central duct connecting to **chambers** around cylinder **liners** via cast-in **ports**.

DC Q51 Q52

IN MEZGER, H

PA (HARL-N) HARLEY-DAVIDSON MOT; (PORS) PORSCHE AG F

CYC 5

PI DE 3326317 A 19850131 (198506)* 12p

GB 2143583 A 19850213 (198507)

FR 2549536 A 19850125 (198510)

US 4530315 A 19850723 (198532)

GB 2143583 B 19870204 (198705)

DE 3326317 C 19880922 (198838)

IT 1176400 B 19870818 (199031)

ADT DE 3326317 A DE 1983-3326317 19830721; GB 2143583 A GB 1984-16315 19840627; US 4530315 A US 1984-630704 19840713

PRAI DE 1983-3326317 19830721

IC F01P003-02; F02B075-22; F02F001-14; F02F007-00

AB DE 3326317 A UPAB: 19930925

The one-piece pressure-cast cylinder block (1) is for a water-cooled i.c. engine with two rows (2,3) of cylinders (10,12)

arranged in V-formation. It contains a longitudinal coolant feed duct (4). This duct connects with the annular coolant spaces (6) of the individual cylinders which are arranged between cylinder **liners** and outer cylinder walls (17).

The duct extends centrally in the block between the two rows and connects to the coolant spaces via **radial ports**

(14,16). These are arranged in the wall and produced by approp. cores during casting.

ADVANTAGE - Positive cooling of cylinder portions subject to high thermal load. Coolant duct and connections are produced by reusable cores in the pressure casting, no subsequent finishing work, blanking plugs or covers being required.

1/5

ABEQ DE 3326317 C UPAB: 19930925

The integral cylinder block for a water-cooled i.c. engine has two rows of cylinders in a V. A longitudinal passage (4) of trapezoidal cross section guides the cooling water to the cylinders. The passage lies in a vertical plane which passes through the crankshaft centre line and extends between the cylinder rows.

The passage is connected by openings in the side walls (17) to the cooling spaces for the cylinders. A U-shaped passage (24) in the side wall connects to the openings in the trapezoidal passage. A section of the U-shaped passage extends parallel to the cylinder centre lines and connects to the coolant spaces round the cylinders.

ADVANTAGE - Effective cooling of high thermal load. Sections of the cylinders.

ABEQ GB 2143583 B UPAB: 19930925

A one-piece cylinder block for a water-cooled internal combustion engine with two rows of cylinders in a V formation, in particular produced by diecasting, there being provided a longitudinally extending coolant supply duct connected to the coolant spaces of the cylinders, said spaces extending between the cylinder sleeves and an outer wall of the block, wherein the longitudinally extending duct is disposed between the rows of cylinders in the cylinder block, at least one opening being provided for each cylinder cooling space and cast in a wall of the cylinder block disposed directly adjacent the longitudinal duct, each opening extending radially to its associated cylinder.

ABEQ US 4530315 A UPAB: 19930925

The one-piece cylinder block, for a water-cooled I.C. engine with two rows of cylinders in a V-arrangement, has a longitudinal duct for supplying cooling water. The block is pref. made by a die-casting process. The longitudinal duct is connected to the coolant spaces of the cylinders which are located between a cylinder sleeve and an outer jacket surrounding the latter.

The longitudinal duct is disposed between the rows of cylinders in the cylinder block. At least one opening is provided in the region of the coolant spaces for each cylinder. The openings are cast in the casing walls of the cylinder block. Since they are disposed directly adjacent the longitudinal duct, they extend radially to the cylinders.

ADVANTAGE - Selective cooling can be provided to the regions of the cylinders which are subjected to high heat stress.

FS GMPI
FA AB

AN 1984-154392 [25] WPIX
 DNN N1984-114715 DNC C1984-064983
 TI Wafer surface coating - by placing it in reaction chamber
 fed with reactive gas.
 AW CVD CHEMICAL VAPOUR DEPOSIT.
 DC L03
 PA (HEWP) HEWLETT-PACKARD CO; (YOKH) YOKOGAWA HEWLETT PACKARD LTD
 CYC 2
 PI JP 59056576 A 19840402 (198425)* 12p
 US 4696833 A 19870929 (198741)
 ADT JP 59056576 A JP 1983-153999 19830323; US 4696833 A US 1985-794311
 19851030
 PRAI US 1982-412327 19820827; US 1985-794311 19851030
 IC C23C011-00; H01L021-20
 AB JP 59056576 A UPAB: 19930925

Wafer is placed in a reaction chamber and reactive gas is introduced through a pipe having one end connected to a gas source and the other end placed in the vicinity of the wafer.

The method is suitable for uniformly forming a coating film on a wafer to mfr. an integrated circuit having mutual junctions of 1 micron in width. Since reactive gas is introduced in the vicinity of the wafer, the conc. of said gas near the wafer is uniform. Hence, the precipitation of a CVD prod. on to the wafer is performed at a controlled reaction speed.

0/9

ABEQ US 4696833 A UPAB: 19930925
 In the chemical vapour deposition

coating of integrated circuit wafers reactant gases are supplied into a chamber enclosed by a wall having a cylindrical sidewall and two end walls.

The vol. contg. the wafers is encircled with a cylindrical liner adjacent to the edges of the wafer to reduce the amt. of reactant prods. on the sidewall and prevent deposits falling on the wafers.

At least one reactant gas is supplied as jets directed against the inside of the liner before the jets pass into the vicinity of the wafers, so that turbulence is produced which mixes the gases. The jets have the same circumferential direction about the liner axis so that a net rotational motion occurs around the edges of the wafers.

ADVANTAGE - Highly uniform coatings are produced for integrated circuits with interconnect lines approx. 1 micron in width.

FS CPI
 FA AB
 MC CPI: L03-D03

L165 ANSWER 40 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1984-035427 [06] WPIX
 DNN N1984-026657 DNC C1984-015103
 TI Tubular electric resistance furnace - has L-shaped heating tube of silicon with bend featuring discharge port coaxial with

charge port.

DC J08 M24 Q77
 IN ALFEROV, Y U E; MIKLIN, V G; PASHIN, Y U D
 PA (SAAG-R) SARAT AGRIC MECH; (SAEL-R) SARAT ELECTROTHERM EQPT
 CYC 1
 PI SU 1006888 A 19830323 (198406)* 3p
 ADT SU 1006888 A SU 1980-2997556 19801014
 PRAI SU 1980-2997556 19801014
 IC F27B005-04; F27B009-08
 AB SU 1006888 A UPAB: 19930925

Improved heat treatment of blanks is achieved with the electric tubular resistance furnace due to increased temp. at its outlet end, and this is combined with improved coefficient of power utilization. The unit has a lined working chamber with handling ports, as well as a heating tube made of silicon with cooled current leads wrapping the ends of the tube. The heating tube is L-shaped and its discharge port is at the bend and coaxially set with the charge port.

The heating of blanks is due to heat conduction and radiation while moving along the tube (3) the ends of which project outside the casing (1). The ends are wrapped by the water cooled current conductors (5,6), and heat losses are reduced by slide gate (7) opened only for discharge. Bul.11/23.3.83

2/2

FS CPI GMPI
 FA AB
 MC CPI: J09-A; M24-D04; M29-C02

L165 ANSWER 41 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1983-34237K [14] WPIX
 DNN N1983-061684 DNC C1983-033443
 TI Furnace for rapid heating of blanks before processing - contains nozzles of burners connected into uniform slit along final heating zone.

DC M24 Q77
 IN PAVLETISOV, Y U S; POPOV, V S; STRIGA, V F
 PA (TEPP) SVERD TEPLOPROEKT

CYC 1
 PI SU 932166 B 19820530 (198314)* 3p
 PRAI SU 1980-3219474 19801217
 IC F27B003-22; F27B009-22
 AB SU 932166 B UPAB: 19930925

Increased intensity of heating ferrous and non-ferrous blanks as prepn. for forging, rolling, squeezing and similar plastic processes in metallurgical, general engineering and metal working industries, and simplified construction of the rapid heating furnace are ensured. The furnace for heating by convection contains jacket (1) with refractory lining (2), working chamber divided into zones of preliminary and final heating (3 and 4 resp.) and nozzle in the form of a slit.

The blanks to be heated are loaded on the sole (6). The fuel is

fed under pressure through a pipeline to burners, and the air through another pipeline. The stream of combustion gases formed by the slit nozzle (5) flows directly onto the surface of the blanks in zone (4) of final heating. After performing preliminary heating of blanks in zone (3), the gases are discharged by a flue. Bul.20/30.5.82.

1/2

FS CPI GMPI

FA AB

MC CPI: M21-N04; M24-D04; M29-C02

L165 ANSWER 42 OF 42 WPIX (C) 2002 THOMSON DERWENT

AN 1980-36696C [21] WPIX

TI Chemical vapour deposition rig - with cold gas quenching compartment above induction heated susceptor.

DC L02 M13 P32

IN HIEBER, K; POLITYCKI, A; STOLZ, M

PA (SIEI) SIEMENS AG

CYC 6

PI DE 2849240 A 19800514 (198021)*

EP 11148 A 19800528 (198022) DE

R: AT CH FR SE

US 4258658 A 19810331 (198116)

EP 11148 B 19811014 (198143) DE

R: AT CH FR SE

DE 2849240 C 19830113 (198303)

PRAI DE 1978-2849240 19781113

REP AT 288811; DE 2218609; DE 2539434; GB 1356769; US 3796182

IC A61C001-05; C23C011-00

AB DE 2849240 A UPAB: 19930902

Small components such as clamping elements for dental drills and turbines are coated with wear-resistant linings e.g. of titanium carbide or titanium nitride by a chemical vapour deposition technique. A jacketed reactor has on top an axially adjustable and rotatable gas supply tube and two thermocouples for temp. control.

After the deposition has been completed, the frame with the mesh discs carrying the components is extracted from the h.f. heated susceptor and exposed to a cooling air stream.

This integrates the quenching operation with the depositing operation and saves a separate process. The circulation of hot oil through the jacket prevents the deposition of condensates on the reactor walls which may lead to flash-overs.

FS CPI GMPI

FA AB

MC CPI: L02-J01E; M13-E02

=> d 1173 1-12 ti

L173 ANSWER 1 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Gas distribution system for s semiconductor substrate

processing has a showerhead and a gas distribution chamber with a contoured surface for providing desired gas pressure distribution at the showerhead.

L173 ANSWER 2 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI High density plasma chemical vapor deposition tool for depositing films onto semiconductor substrates includes a remote plasma chamber cleaning system.

L173 ANSWER 3 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Chemical processing microsystem has microreactors with reaction cavities loaded with materials that are accessible for loading and unloading material content laminate respectively before and after reaction.

L173 ANSWER 4 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Treating a substrate material or film present on the material surface in an anisotropic manner, in particular treating a semiconductor wafer.

L173 ANSWER 5 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Liquid vaporiser system for introduction of liquids into a CVD apparatus - with improved control of stoichiometric rate of deposition..

L173 ANSWER 6 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Apparatus for controlled heating of semiconductor wafers in sealed environment - has heating lamps in transparent tubes allowing rapid heating and cooling.

L173 ANSWER 7 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Temp. controlled shower-head discharge assembly - for chemical vapour deposition using a discharge head with heat exchange passages, to provide a controlled isothermal temp..

L173 ANSWER 8 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Hydrogen fluoride recovery from sulphuric acid or gas contg. fluoride - by spraying acid in countercurrent to gas into reactor with various temp. zones and continuous discharge of gas and acid.

L173 ANSWER 9 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Reactant gas distributor for glass sheet chemical vapour deposition - providing temp. control for uniform coating, has plenum for each gas surrounded by coolant duct and heaters.

L173 ANSWER 10 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI CVD appts. for coating glass - includes 2 plenum chambers for deposition gases and mixing chamber

for the gases with outlet adjacent deposition surface.

L173 ANSWER 11 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Heat treatment furnace e.g. for semiconductor wafers - has substrate inserted into furnace on carrier together with thermoelement.

L173 ANSWER 12 OF 12 WPIX (C) 2002 THOMSON DERWENT

TI Multi-purpose reactor - for processing single semiconductor wafer at high rate, providing plasma-enhanced reactions and uniform gas flow.

=> d l173 1,4,6,7,9,10,12 max

L173 ANSWER 1 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 2001-138191 [14] WPIX

DNN N2001-100607 DNC C2001-040714

TI Gas distribution system for semiconductor substrate processing has a showerhead and a gas distribution chamber with a contoured surface for providing desired gas pressure distribution at the showerhead.

DC L03 U11

IN DHINDSA, R; HAO, F

PA (LAMR-N) LAM RES CORP

CYC 93

PI WO 2001003163 A1 20010111 (200114)* EN 27p H01L021-00

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC
MW MZ NL OA PT SD SE SL SZ TZ UG ZW

W: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK
DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL
PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU
ZA ZW

AU 2000054837 A 20010122 (200125) H01L021-00

US 6415736 B1 20020709 (200253) C23C016-00

ADT WO 2001003163 A1 WO 2000-US16143 20000612; AU 2000054837 A AU
2000-54837 20000612; US 6415736 B1 US 1999-343481 19990630

FDT AU 2000054837 A Based on WO 200103163

PRAI US 1999-343481 19990630

IC ICM C23C016-00; H01L021-00

ICS H05H001-00

AB WO 200103163 A UPAB: 20010312

NOVELTY - The gas distribution system includes a support body (20), gas distribution chamber (24), gas supply inlet (102), showerhead (22), and contoured surface (94) in the gas distribution chamber. The contoured surface provides a desired gas pressure distribution at the backside of the showerhead.

DETAILED DESCRIPTION - The gas distribution system includes a support body, gas distribution chamber, gas supply inlet through which pressurized process gas flows into the distribution chamber, showerhead, and contoured surface in the gas distribution chamber.

The showerhead is supported by the support body such that the pressurized process gas in the gas distribution chamber applies pressure to a backside of the showerhead and passes through openings extending between the backside and opposite side of the showerhead.

The contoured surface provides a desired gas pressure distribution at the backside of the showerhead.

An INDEPENDENT CLAIM is also included for a method of processing a substrate in a reaction chamber containing the gas distribution chamber.

The method includes supplying a semiconductor substrate to the reaction chamber, flowing process gas through the gas supply inlet and into a region above the semiconductor substrate, and processing the wafer with the process gas.

USE - For processing semiconductor substrates such as integrated circuit wafers.

ADVANTAGE - The system results to a uniform distribution of gas to the backside of the showerhead, increasing the consistency and yield of the process for the manufacture of semiconductor substrates.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of gas distribution chamber with a contoured surface.

Support body 20

Coolant channel 21

Showerhead 22

Gas distribution chamber 24

Lower plenum 24a

Baffle plate 92

Contoured surface 94

Central portion 98

Baffle plate openings 100

Gas supply inlet 102

Dwg.3A/5

TECH WO 200103163 A1UPTX: 20010312

TECHNOLOGY FOCUS - MECHANICAL ENGINEERING - Preferred Component: The contoured surface comprises nonplanar upper and/or lower surface of a baffle plate (92). The gas distribution chamber has upper and lower plenum (24a) above and below the baffle plate, respectively. The gas inlet supplies the process gas through an inlet which opens into an outer region of the upper plenum and a central opening in a planar surface facing the baffle plate.

The baffle plate is conical and has a thickness which is larger in a central portion (98) and smaller at an outer portion. The baffle plate has openings (100) which are longer in a central portion of the baffle plate and shorter in an outer portion of the baffle plate.

The support body includes a coolant channel (21) and a second gas supply inlet which supplies process gas that passes through the baffle plate.

The showerhead is a showerhead electrode of a plasma chamber

The support member comprises a **temperatur - controlled** member.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Semiconductor Substrate:

The semiconductor substrate comprises a **silicon wafer**.

Preferred Method: **Etching** of a layer on a semiconductor substrate is done by supplying radio frequency power to the showerhead electrode such that the process gas forms a plasma in contact with an exposed surface of the **semiconductor** substrate. The **etching** step is carried out as a part of the process of manufacturing a damascene **structure**. It includes etching openings through exposed portions of a dielectric layer on the substrate to an electrically (semi)conductive layer on the substrate.

FS CPI EPI

FA AB; GI

MC CPI: L04-D

EPI: U11-C07A1; U11-C09B; U11-C09C

L173 ANSWER 4 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 2000-171482 [15] WPIX

CR 1999-601259 [51]; 2000-587267 [55]; 2000-~~58~~7343 [55]; 2000-601859 [57]

DNN N2000-127404 DNC C2000-053474

TI Treating a substrate material or film **present** on the material surface in an anisotropic manner, in particular **treating** a **semiconductor wafer**.

DC A85 L03 U11

IN BHARDWAJ, J K

PA (SURF-N) SURFACE TECHNOLOGY SYSTEMS LTD; (SURF-N) SURFACE TECHNOLOGY SYSTEMS PLC

CYC 22

PI WO 2000005749 A2 20000203 (200015)* EN 40p H01L021-00
RW: AT BE CH CY DE DK ES FI FR GB GR ~~IE~~ IT LU MC NL PT SE
W: JP KR US

EP 1099244 A2 20010516 (200128) EN H01L021-306
R: AT BE CH CY DE DK ES FI FR GB GR ~~IE~~ IT LI LU MC NL PT SE

KR 2001072054 A 20010731 (200208) H01L021-3065

JP 2002521814 W 20020716 (200261) 42p H01L021-306

ADT WO 2000005749 A2 WO 1999-GB2368 19990723; EP 1099244 A2 EP 1999-934921 19990723, WO 1999-GB2368 1999~~0~~723; KR 2001072054 A KR 2001-701053 20010126; JP 2002521814 W WO 1999-GB2368 19990723, JP 2000-561646 19990723

FDT EP 1099244 A2 Based on WO 200005749; JP 2002521814 W Based on WO 200005749

PRAI GB 1999-11401 19990518; GB 1998-15931 19980723; GB 1998-23364 19981027; GB 1999-4925 19990304; GB 1999-10725 19990511

IC ICM H01L021-00; H01L021-306; H01L021-306~~5~~

ICS H01L021-311; H01L021-3213

AB WO 200005749 A UPAB: 20020924

NOVELTY - A substrate material or film **present** on the material surface is treated by:

- (a) etching the material or film;
- (b) depositing or forming a passivation layer on the surfaces of an etched feature; and
- (c) selectively removing the passivation layer from the etched feature in order that the etching proceeds in a direction perpendicular to the material of film surface.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for an apparatus used for the process comprising a chamber (15) having a chemical inlet (13) and chemical outlet (14) in which is positioned a support for receiving a substrate (17). The apparatus further comprises an etching device, a depositing device and a device for selectively removing the passivation layer from the etched feature.

USE - For treating a substrate material or film present on the material surface in an anisotropic manner, in particular treatment of semiconductor wafer.

ADVANTAGE - Allows the cyclic etch passivation technique to be used with materials that are not necessarily best etched by plasma means in that unacceptable low etch rates result.

DESCRIPTION OF DRAWING(S) - The figure shows a diagrammatic view of an apparatus for carrying out the etching step.

Apparatus 12

Inlet port 13

Outlet port 14

Chamber 15

Electrode 16

Substrate 17

Dwg.1/11

TECH WO 200005749 A2UPTX: 20000323

TECHNOLOGY FOCUS - METALLURGY - Preferred Method: Step (a) is performed with one or more chemicals in the absence of plasma. The other of steps (a) and (b) is performed in the presence of a plasma. The material of film is etched with hydrogen fluoride (HF), nitric acid (HNO₃) and acetic acid (CH₃COOH), or with a halogen containing compound, preferably an inter-halogen gas. Water and/or an alcohol is present in step (a). The material or film can be etched using an aqua regia. Nitrogen or other inert gas is present in step (a) and/or is used as a purging gas between the steps of the method. The passivation layer is formed on a surface that is resistant to chemical etched. The passivation layer is deposited using a polymer. When plasma is not present in step (b), a photo-enhanced polymerization process is used in the deposition of the passivation layer. The selective removal of the passivation layer is carried out by surface irradiation. The irradiation is thermal heating of either the front and/or the rear surface of the material or film to provide thermolytic decomposition, or is provided by a light source on the front of the material or film resulting in photolytic decomposition, or where the irradiation source is an excimer laser. It is directional or collimated parallel to the direction of etch front propagation. The surface irradiation is a plasma where the ion energy is preferably greater than 10 eV. Any gases employed are delivered from a point of use delivery system positioned locally to

a **chamber** within which the method is performed. The process is operated at pressures above atmosphere and/or at elevated temperature using an etchant materials any one or more of diketones, ketoimines, halogenated-carboxylic acid, **acetic acid**, and formic acid chemistries and extensions including hexafluoro-2,4-pentadione and other fluorinated acetyl-acetone groups.

Preferred Components: The material surface has previously had a defined mask pattern. The material or film is a dielectric, which is an oxide, preferably of silicon, quartz, **glass**, pyrex, silicon dioxide (SiO₂) deposited by chemical vapor deposition (CVD), or SiO₂ grown by

thermal, plasma or other means to deposit or grow the oxide. The plasma comprises a precursor gas or mixture of precursor gases. The precursor gas comprises an inert gas that is capable of physically removing the passivation layer and/or a gas that is capable of physically removing the passivation layer with chemical enhancement. It comprises an etchant chemical used in step (a) or a material used for depositing the passivation layer in step (b).

Preferred Apparatus: The support is in the form of a first electrode and preferably also a second electrode that is spaced from the first electrode. The apparatus further comprises a device for providing radio frequency (RF) energy or microwave energy to a plasma in the **chamber**. It further comprises an electrical device for providing an electrical bias on to the support to accelerate ions onto the substrate for at least part of the cycle. It further comprises a radiating device for providing radiation energy into the **chamber**, and/or means for controlling the substrate temperature, and/or rotator for enhancing the homogeneity of the etching. The apparatus is associated with a single **chamber**.

TECHNOLOGY FOCUS - POLYMERS - The polymer is of formula: $n(C_xF_y)$
X and Y = any suitable values.

ABEX WO 200005749 A2UPTX: 20000323

SPECIFIC MATERIALS - The material of film is a conductor, preferably a gold (Au) or platinum (Pt), or a semiconductor, preferably a silicon (Si), silicon germanium (SiGe) or germanium (Ge).

FS CPI EPI

FA AB; GI

MC CPI: A11-B05C; A12-E07C; L04-B04; L04-C07

EPI: U11-C05B9A; U11-C07A1; U11-C07A2

PLE UPA 20001114

[1.1] 018; G1978-R D01 7A G1990 G1978; P1854; P0500 F- 7A;
H0000; H0011-R; L9999 L2506-R; L9999 L2562 L2506; L9999
L2299; K9790-R

[1.2] 018; ND01; ND03; ND07; N9999 N7158 N7034 N7023; N9999
N7147 N7034 N7023; K9687 K9676; K9712 K9676; K9483-R;
Q9999 Q7114-R; Q9999 Q7476 Q7330

L173 ANSWER 6 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 1997-310166 [28] WPIX

DNN N1997-257039 DNC C1997-099695

TI Apparatus for controlled heating of semiconductor wafers in sealed environment - has heating lamps in transparent tubes allowing rapid heating and cooling.

DC L03 Q76 Q77 U11

IN KOTECKI, D E; NATZLE, W C; YU, C

PA (IBMC) INT BUSINESS MACHINES CORP

CYC 1

PI US 5636320 A 19970603 (199728)* 6p H01L021-205

ADT US 5636320 A US 1995-452466 19950526

PRAI US 1995-452466 19950526

IC ICM H01L021-205

ICS F26B019-00; F27D001-00

AB US 5636320 A UPAB: 19970709

An apparatus for **controlled temperature**

treatment of a batch of semiconductor wafers in a sealed environment comprises a sealed **chamber** with **inlet** (104) and **outlet** (106) **ports** and a wall for receiving the wafers (110). There is a tube (108) for receiving a heating means (200) which passes into the **chamber** without a break of seal, a tube cooling means (112) having a rapid disconnect and a means of cooling the **chamber** wall.

Also claimed is a method of controllably heating the wafers using the apparatus above comprising admitting reactant gas into the **chamber** and cooling the **chamber** walls during the reaction, which leaves a residue on the wafer removable by desorption. The wafer/**chamber** **temperature** is **controlled** during reaction and the workpiece is subsequently heated to desorb the residue.

USE - In vapour processing of semiconductor wafers in heated reactors, e.g., during etching

ADVANTAGE - Wafer heating and cooling are rapid so that wafer batch processing is efficient: the **chamber** can be readily serviced without interruption.

Dwg.1/5

FS CPI EPI GMPI

FA AB; GI

MC CPI: L04-C16; L04-D

EPI: U11-C03J2A; U11-C09X

L173 ANSWER 7 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 1996-433850 [43] WPIX

DNC C1996-136250

TI **Temp. controlled** shower-head discharge assembly

- for **chemical vapour deposition** using

a discharge head with heat exchange passages, to provide a **controlled** isothermal temp..

DC L03 M13

IN VAN, BUSKIRK P C

PA (ADTE-N) ADVANCED TECHNOLOGY MATERIALS

CYC 20

PI WO 9628585 A1 19960919 (199643)* DE 36p C23C016-00

RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

W: JP KR

US 5653806 A 19970805 (199737) 13p C23C016-00

ADT WO 9628585 A1 WO 1996-US3131 19960308; US 5653806 A US 1995-402142 19950310

PRAI US 1995-402142 19950310

REP JP 6332929; US 3098763; US 4313783; US 5000113; US 5273588; US 5387289; US 5462014; WO 9010092

IC ICM C23C016-00

AB WO 9628585 A UPAB: 19961025

Appts. for dispersing a vapour phase reagent material onto a substrate (98,99), where the vapour phase reagent contains the deposition species and must be controlled to within a narrow temp. range to avoid condensation or decomposition. The disperser includes a housing (52) in communication with reagent source, the housing having a wall (81) defining the discharge face (80). The wall has a number of spaced apart discharge passages (82) which are heated by a number of heat exchange passages also disposed in the wall. Also claimed is the disperser used in chemical vapour deposition where, a temp. sensor and controller maintains the discharge nozzle controlling the heat exchange medium flow and the substrate is mounted in a chemical vapour deposition chamber 2-25 cm away from the nozzle.

USE - Used for delivering a vapour phase reagent to a substrate in a chemical vapour deposition reactor.

ADVANTAGE - Used for dispersing a reagent to a substrate at an accurate and isothermal (within plus or minus 10 deg.C) temper avoiding decomposition and condensation of temperature sensitive reagents. This invention can for example disperse the reagent at temperatures as low as 150 deg.C when the substrate at 700 deg.C and disposed 2 cm from the discharge face.
Dwg.5/8

ABEQ US 5653806 A UPAB: 19970915

An equipment for dispersingly delivering a vapour-phase source reagent material containing a deposition species, to a substrate for deposition of the deposition species on it. The temperature of the dispersed source reagent vapour must be controllably maintained within a relatively narrow range of temperature in order to avoid substantial occurrence of either premature condensation of the source reagent vapour prior to the deposition on the substrate, caused by excessively low source reagent temperatures, or decomposition of the source reagent vapour, caused by excessively high vapour temperatures. The equipment comprises: (a) a disperser including a housing enclosing an interior volume within it, where the housing is joinable in flow communication with a supply of source reagent vapour so that source reagent vapour from it is flowable into the interior volume of the housing, the housing comprising a wall defining a discharge face of the disperser, the wall having an array of discharge passages in it for discharge of the source reagent vapour to a substrate in close proximity to the wall and in source reagent vapour-receiving relationship to it, the

discharge passages being in spaced-apart relationship to one another, forming a geometrically regular array of parallel rows of source reagent discharge passage openings at the discharge face, the discharge passage openings extending through the wall; and (b) a manifold heat exchange assembly integrally formed in the housing wall, the manifold heat exchange assembly comprising inlet and outlet manifolds joined in closed flow communication with one another by heat exchange medium branch passages in the housing wall, in transversely spaced-apart, parallel relationship to one another and to the rows of discharge passage openings in the wall, and disposed in heat transfer relationship to the source reagent vapour discharge passages in the housing wall, with each of the heat exchange medium branch passages being in spaced-apart heat transfer relationship to a multiplicity of source reagent vapour discharge passages in the array, such that the number and form of the heat exchange medium branch passages provide effective heat exchange to the entire surface of the wall of the housing, and such that the discharge passages extending through the wall are not occluded by the heat exchange medium branch passages.

Dwg.0/8

FS CPI
FA AB; GI
MC CPI: L04-D01; M13-E07

L173 ANSWER 9 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 1991-360971 [49] WPIX

CR 1988-353964 [49]

DNN N1991-276555 DNC C1991-155602

TI Reactant gas distributor for glass sheet chemical vapour deposition - providing temp. control for uniform coating, has plenum for each gas surrounded by coolant duct and heaters.

DC L01 X25

IN BAUMAN, R L; GREENBERG, W M

PA (LIBY) LIBBEY OWENS FORD CO

CYC 1

PI US 5065696 A 19911119 (199149)*

ADT US 5065696 A US 1990-489002 19900306

PRAI US 1987-50466 19870518; US 1988-245444 19880916; US 1990-489002 19900306

IC C23C016-00

AB US 5065696 A UPAB: 19950301

Appts. for depositing a coating on the surface of glass sheet includes two plenums receiving separate resistant gases, each discharging is a common mixing chamber having a discharge outer adjacent to the sheet surface. The chamber is defined by the walls of blocks of material of high thermal conducting.

A support structure incorporates a coolant fluid duct and thermal insulation material is placed between the blocks and the support and between the plenums and the support. The plenums, blocks and insulation are attached to the support

by cooled threaded fasteners extending through the blocks into the support and having a high coefft. of thermal conductivity; the shank of the fastener passes through a bushing of thermally insulating material extending from the head to the support.

USE/ADVANTAGE - Coating moving ribbon of hot glass by **chemical vapour deposition**. Close **control** of the **temp.** of the reactant gases giving uniformity of coating. @(6pp Dwg.No.4/5)@
4/5

FS CPI EPI
FA AB; GI
MC CPI: L01-G04C
EPI: X25-A04

L173 ANSWER 10 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 1988-353964 [49] WPIX

CR 1991-360971 [49]

DNC C1988-156604

TI CVD appts. for coating glass - includes 2 **plenum chambers** for deposition gases and mixing **chamber** for the gases with outlet adjacent deposition surface.
CHEMICAL VAPOUR DEPOSIT.

AW

DC L01 M13 P42

IN BAUMAN, R L; GREENBERG, W M; MAAS, D

PA (LIBY) LIBBEY OWENS FORD CO

CYC 19

PI WO 8809394 A 19881201 (198849)* EN 23p

RW: BE CH DE FR GB IT LU NL SE

W: AU BR FI JP KR

US 4793282 A 19881227 (198903) 9p

ZA 8803485 A 19890222 (198914)

AU 8817887 A 19881221 (198916)

EP 316409 A 19890524 (198921) EN

R: BE CH DE FR GB IT LI LU NL SE

FI 8900226 A 19890117 (198940)

BR 8807160 A 19891017 (198947)

ES 2008499 A 19890716 (198948)

JP 01503295 W 19891109 (198951)

CA 1293119 C 19911217 (199206)

EP 316409 A4 19891011 (199507)

ADT WO 8809394 A WO 1988-US1578 19880512; US 4793282 A US 1987-50466

19870518; EP 316409 A EP 1988-904883 19880512; ES 2008499 A ES

1988-1533 19880517; JP 01503295 W JP 1988-504596 19880512; EP 316409

A4 EP 1988-904883

PRAI US 1987-50466 19870518

REP US 3850679; FR 2314152; FR 2518429

IC B05C011-00; C03C017-09; C23C016-00

AB WO 8809394 A UPAB: 19950301

CVD appts. for coating a sheet of glass comprises: two separate **chamber** for receiving first and second coating gases, with a septum between the two **chamber**; a mixing **chamber** connected to the outlets of the two **chambers**

and having an outlet adjacent the glass surface; and a mixing device in the mixing chamber to provide a coating compsn. for the mixing chamber outlet.

Temp. control devices are pref. provided in the two initial chambers, pref. a thermocouple and cooling ducts and/or a heater.

USE/ADVANTAGE - In coating a moving ribbon of lat glass. Appts. permits precise process control, esp. in gas mixing and in temp. of the mixed gas.

0/4

Dwg.0/4

ABEQ US 4793282 A UPAB: 19930923

Distributor beam for coating flat glass includes an inverted U-shaped channel, within which is another inverted U-shaped channel, joined to the first by horizontal members, defining a duct for heat transfer fluids, attached by blocks, one forming a heater, defining an outlet passage for gas. U-shaped channel members form adjacent plenums receiving coating gases which passes into a mixing chamber and contact a finger baffle extending across the width of the chamber, splitting gas streams into multiple streams for mixing.

ADVANTAGE - Uniform gas distribution with heating and cooling for temp. control.

FS CPI GMPI

FA AB

MC CPI: L01-G04C; M13-E07

L173 ANSWER 12 OF 12 WPIX (C) 2002 THOMSON DERWENT

AN 1988-169404 [25] WPIX

CR 1989-001340 [01]; 1992-009935 [02]

DNN N1988-129539 DNC C1988-075497

TI Multi-purpose reactor - for processing single semiconductor wafer at high rate, providing plasma-enhanced reactions and uniform gas flow.

DC L03 P42 P78 U11 V05

IN ADAMIK, J A; COLLINS, K S; LAW, K S; LEUNG, C; MAYDAN, D; PERLOV, I; UMOTOY, S P; WANG, D N; WHITE, J M; WANG, D N K

PA (MATE-N) APPLIED MATERIALS INC; (MATE-N) APPL MATERIALS INC

CYC 15

PI EP 272140 A 19880622 (198825)* EN 24p

R: AT BE CH DE ES FR GB GR IT LI LU NL SE

JP 63246829 A 19881013 (198847)

US 4872947 A 19891010 (198950) 21p

US 4892753 A 19900109 (199010) 22p

US 5000113 A 19910319 (199114) 23p

EP 272140 B1 19940223 (199408) EN 29p C23C016-54

R: AT BE CH DE ES FR GB GR IT LI LU NL SE

JP 06013367 A 19940121 (199408) 19p H01L021-31

JP 06013368 A 19940121 (199408) 19p H01L021-31

JP 06012771 B2 19940216 (199410) H01L021-31

DE 3789142 G 19940331 (199414) C23C016-54

ES 2049729 T3 19940501 (199421) C23C016-54

US 5354715	A	19941011 (199440)	21p	H01L021-00
US 5362526	A	19941108 (199444)	24p	B05D003-06
JP 08055843	A	19960227 (199618)	18p	H01L021-31
JP 08070035	A	19960312 (199620)	19p	H01L021-68
JP 2584960	B2	19970226 (199713)	19p	H01L021-68
JP 2651102	B2	19970910 (199741)	18p	H01L021-31
JP 2716642	B2	19980218 (199812)	19p	H01L021-316
JP 2723845	B2	19980309 (199815)	18p	H01L021-31
US 5755886	A	19980526 (199828)		C23C016-00
US 5871811	A	19990216 (199914)		C23C016-00
US 36623	E	20000321 (200021)		H05H001-24
US 6167834	B1	20010102 (200103)		C23C016-00

ADT EP 272140 A EP 1987-311193 19871218; JP 63246829 A JP 1987-321181 19871218; US 4872947 A US 1988-262992 19881026; US 4892753 A US 1988-262993 19881026; US 5000113 A US 1986-944492 19861219; EP 272140 B1 EP 1987-311193 19871218; JP 06013367 A Div ex JP 1987-321181 19871218, JP 1993-38905 19871218; JP 06013368 A Div ex JP 1987-321181 19871218, JP 1993-38904 19871218; JP 06012771 B2 JP 1987-321181 19871218; DE 3789142 G DE 1987-3789142 19871218, EP 1987-311193 19871218; ES 2049729 T3 EP 1987-311193 19871218; US 5354715 A Div ex US 1986-944492 19861219, Div ex US 1991-645999 19910123, US 1992-861719 19920401; US 5362526 A Div ex US 1986-944492 19861219, US 1991-645999 19910123; JP 08055843 A Div ex JP 1993-38904 19871218, JP 1995-201143 19871218; JP 08070035 A Div ex JP 1993-38904 19871218, JP 1995-201144 19871218; JP 2584960 B2 Div ex JP 1993-38904 19871218, JP 1995-201144 19871218; JP 2651102 B2 Div ex JP 1987-321181 19871218, JP 1993-38904 19871218; JP 2716642 B2 Div ex JP 1987-321181 19871218, JP 1993-38905 19871218; JP 2723845 B2 Div ex JP 1993-38904 19871218, JP 1995-201143 19871218; US 5755886 A Cont of US 1986-944492 19861219, Cont of US 1990-537445 19900613, Cont of US 1992-928642 19920813, US 1995-483750 19950607; US 5871811 A Cont of US 1986-944492 19861219, Cont of US 1990-537445 19900613, Cont of US 1992-928642 19920813, US 1995-477536 19950607; US 36623 E Div ex US 1986-944492 19861219, US 1988-262993 19881026, Cont of US 1995-407482 19950316, US 1996-752972 19961202; US 6167834 B1 Cont of US 1986-944492 19861219, Cont of US 1990-537445 19900613, US 1992-928642 19920813

FDT JP 06012771 B2 Based on JP 63246829; DE 3789142 G Based on EP 272140; ES 2049729 T3 Based on EP 272140; US 5354715 A Div ex US 5000113; US 5362526 A Div ex US 5000113; JP 2584960 B2 Previous Publ. JP 08070035; JP 2651102 B2 Previous Publ. JP 06013368; JP 2716642 B2 Previous Publ. JP 06013367; JP 2723845 B2 Previous Publ. JP 08055843; US 5755886 A Cont of US 5000113; US 5871811 A Cont of US 5000113; US 36623 E Reissue of US 4892753, Div ex US 5000113; US 6167834 B1 Cont of US 5000113

PRAI US 1986-944492 19861219; US 1988-262992 19881026; US 1991-645999 19910123; US 1992-861719 19920401; US 1990-537445 19900613; US 1992-928642 19920813; US 1995-483750 19950607; US 1995-477536 19950607; US 1995-407482 19950316; US 1996-752972 19961202

REP 5.Jnl.Ref; A3...9046; DD 209485; DE 3416470; EP 140755; EP 152555; EP 157052; EP 159621; EP 215968; EP 272141; EP 272142; EP 296891; EP 60917; FR 1490476; FR 2465791; GB 1174755; GB 2104054; GB 2181458;

GB 2181460; No-Sr.Pub; US 3330694; US 3854443; US 4535228; US 4547247; US 4576698; US 4592306; US 4693211; WO 8600938; WO 8707310
 IC B05D003-06; B44C001-22; C03C015-00; C03C025-06; C23C016-54; H01L021-31

ICM B05D003-06; C23C016-00; C23C016-54; H01L021-00; H01L021-31; H01L021-316; H01L021-68; H05H001-24

ICS B44C001-22; C03C015-00; C03C025-06; C23C016-40; C23C016-42; C23C016-44; C23C016-46; C23C016-48; C23C016-50; C23F004-00; C30B025-14; H01L021-02; H01L021-205; H01L021-3065

AB EP 272140 A UPAB: 20010116

A chemical vapour deposition

reactor comprises a **chamber** hving an **inlet**

manifold for reaction gases which has **temp.**

controlled inner and outer surfaces for enhanced deposition

control and presentation of deposition within it. Pref. connected to

the manifold there is a combined RF/gas feed through device

comprising a tube earthed at the **inlet** end and is a RF

supply at the manifold end, the tube having a controlled impedance

along the length is produce-constant voltage gradient and carrying a

coaxial flow of outer purge gas stream and inner deposition gas stream.

Other feastures include a gas distributor plate mounted baove a **wafer** to be **treated** and an exhaust system

providing controlled radial flow of gas over it, together with a mechanism for positioning the wafer in the **chamber**. There

is independently claimed a process for depositing a conformal layer

of silica from a mixture of oxygen, ozone, tetraethyl orthosilicate

and carrier gas using a substrate temp. of 200-500 deg.C and

pressure of 10-200 torr. Also a process of isotropically etching

silica using a plasma formed from NF₃, CF₄ or C₂F₆ at a temp. of

100-500 deg.C and 200 millitorr to 20 torr with an **inlet**

-substrate distance not less than 0.4 cm..

USE/ADVANTAGE - **Processing** single **semi**

conductor wafer by thermal vapour deposition, plasma

enhanced vapour deposition, plasma assisted etch bock, plasma self

cleaning, or sputtering or by a sequence of these. Uniform

deposition over 5-8 inch dia. wafers. High throughput.

Dwg.2/21

Dwg.2/21

ABEQ US 4872947 A UPAB: 19930923

A conformal layer of silicon dioxide is deposited on to a substrate by exposing the substrate to a reactive species formed from ozone, oxygen and tetraethylorthosilicate (I) within a **chamber**.

The pressure within the **chamber** is 10-200 Torr and the

substrate temp. ranges from 200-500 deg.C.

Also new is a process for forming a silicon oxide overlayer on a substrate within a **chamber** by firstly positioning the

substrate within a **chamber** and closely adjacent a manifold

having a multiplicity of closely-spaced **outlet** holes

closely adjacent the substrate. A mixt. comprising ozone, oxygen and

(I) is then applied to the manifold for communicating reactive

nitrogen and oxygen species into the **chamber** via the

outlet holes, while maintaining the substrate within the range 200-500 deg.C and the **chamber** at 10-200 Torr.

USE/ADVANTAGE - Process is provided for forming highly conformal silicon dioxide layers, even over small dimension stepped topographics in VLSI and ULSI devices, using ozone and TEOS gas chemistry and thermal CVD.

ABEQ US 4892753 A UPAB: 19930923

Silicon dioxide is deposited on to a substrate (I) by exposing to plasma formed by a gas mixt. which includes tetraethyl orthosilicate. Firstly, (I) is positioned on a support within a vacuum **chamber** and adjacent within a vacuum **chamber** and adjacent a gas manifold which is an RF electrode and includes a multiplicity of closely-spaced gas **outlets** holes closely adjacent (I). Then the gas mixt. is communicated into the manifold while applying RF energy between the manifold and the substrate support, and maintaining the total pressure, in the **chamber** at 1-50 torr, and the temp. of (I) at 200-500 deg.C. Pref. the gas mixt. includes oxygen.

USE/ADVANTAGE - Highly conformal silicon dioxide layers are formed, even over small dimension stepped topographics in V+SI and ULSI devices, using ozone and TEOS gas chemistry and thermal CVD.

ABEQ US 5000113 A UPAB: 19930923

The **reactor** comprises (a) a housing defining a vacuum **chamber** for mounting a wafer horizontally and including a horizontal **inlet** gas manifold over the wafer mounting position to supply reactant gases, (b) a gas distributor plate mounted peripherally about the wafer mounting position and including a circular array of exhaust holes, (c) a vacuum exhaust pump means, and (d) a circular channel beneath and communicating with the hole array and having an exhaust **port** connected to the vacuum pump means to flow gases radially across the wafer through the exhaust **port**, the channel volume providing high conductance relative to the exhaust holes sufficient to enable controlled radial gas flow across the wafer and thorough the exhaust holes into the channel.

USE/ADVANTAGE - Used for CVD, PECVD, **reactor** self-cleaning film etch back, etc. esp. highly conformal SiO₂ layers even over small dimension stepped topographies in VLSI and ULSI devices even using O₃ and TEOS gas chemistry and thermal CVD. Uniform deposition over a wide range of pressures including very high pressures, excellent conformal coverage eliminating word not edited and voids and in situ multiple step processes in the same **chamber** is possible. @@

ABEQ EP 272140 B UPAB: 19940407

A TEOS-based, plasma enhanced, CVD process for depositing a film of a silicon oxide having improved step coverage onto a surface of a semiconductor wafer having small dimension stepped topographies, such wafer being positioned inside a vacuum **chamber** to receive the silicon oxide,

comprising the steps of:

heating the wafer to a temperature in the range of 200 deg.

C-500 deg. C,
pressurizing the **chamber** to between 133.322 Pa to 666
Pa (1 to 50 Torr);
dispensing toward the wafer a gas mixture which includes an
effective amount of tetraethylorthosilicate ('TEOS') from a
dispensing area which is close to the wafer surface, the gas mixture
being dispensed with a substantially uniform spatial distribution
over the wafer surface; and
applying an effective amount of RF power between the dispensing
area and the wafer, so as to excite the gas mixture into a plasma
state in a thin region between the wafer and the dispensing area;
whereby a layer of silicon oxide having improved step coverage
is deposited onto the wafer.

Dwg.1/21

ABEQ US 5354715 A UPAB: 19941128

A conformal layer of Si oxide is deposited on a substrate by
exposing the surface of the substrate, which is heated to 200-500
deg.C to a plasma of reactive species formed from O₃, O₂ and TEOS
within a **chamber** having a pressure of at least 10 torr.

The TEOS is pref. supplied with He as carrier gas. The Si oxide
is pref. deposited at 500-4000 Angstroms per minute. A P- or
B-contg. gas is pref. added as dopant to the plasma.

USE/ADVANTAGE - Highly conformal SiO₂ layers are formed, even
over small dimension stepped topographies in VLSI and VLSI devices.
Uniform deposition over a wide range of pressures including very
high pressures.

18,19/21

ABEQ US 5362526 A UPAB: 19941223

A TEOS based plasma enhanced **CVD** process for depositing
silicon oxide onto a semiconductor wafer with small dimension
stepped topography.

The wafer is heated in vacuum to 200-500 degrees C before
raising the pressure to 1-50 torr and dispensing a gas mix
containing TEOS (tetraethylorthosilicate) parallel to the wafer
surface. RF power is used to excite the gas to a plasma state in the
work zone. This causes deposition of silicon oxide at a rate above
400 angstroms/mm.

USE/ADVANTAGE - Large scale integrated circuits. Can be used
with densely stepped topographies.

Dwg.1/21

FS CPI EPI GMPI

FA AB; GI

MC CPI: L04-D01; L04-D04

EPI: U11-C05B2; U11-C07A1; U11-C09C; V05-F09

DRN 1779-U

=> file hca

FILE 'HCA' ENTERED AT 17:35:28 ON 04 OCT 2002

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=> d l163 1-20 ti

L163 ANSWER 1 OF 20 HCA COPYRIGHT 2002 ACS

TI Zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment and method of manufacture

L163 ANSWER 2 OF 20 HCA COPYRIGHT 2002 ACS

TI **Chamber liner** for high temperature **processing chamber** for **semiconductor** device fabrication

L163 ANSWER 3 OF 20 HCA COPYRIGHT 2002 ACS

TI Corrosion-resistant protective polymer **lining** for **chamber** apparatus in plasma processing of substrates

L163 ANSWER 4 OF 20 HCA COPYRIGHT 2002 ACS

TI Porous **ceramic liner** for a plasma source

L163 ANSWER 5 OF 20 HCA COPYRIGHT 2002 ACS

TI **Semiconductor processing** equipment having improved particle performance using ceramics

L163 ANSWER 6 OF 20 HCA COPYRIGHT 2002 ACS

TI **Chemical-vapor deposition** **chamber** with substrate processing configurable for deposition or cleaning

L163 ANSWER 7 OF 20 HCA COPYRIGHT 2002 ACS

TI Apparatus and jigs for attachment of polymer moldings as **liners** in manufacture of semiconductor devices

L163 ANSWER 8 OF 20 HCA COPYRIGHT 2002 ACS

TI The development of a combustion **chamber liner** utilizing a long-fiber reinforced composite material made using the polysilazane impregnation method and the **chemical vapor deposition** method

L163 ANSWER 9 OF 20 HCA COPYRIGHT 2002 ACS

TI Method of reducing residue accumulation in **CVD** **chamber** using **ceramic lining**

L163 ANSWER 10 OF 20 HCA COPYRIGHT 2002 ACS

TI Means and method for cleaning **semiconductor wafer** **processing** apparatus

L163 ANSWER 11 OF 20 HCA COPYRIGHT 2002 ACS

TI Ceramic reaction **chamber** with corrosion resistance and heat shock resistance

L163 ANSWER 12 OF 20 HCA COPYRIGHT 2002 ACS

TI Evaluation of plasma surface interaction of boron film used as plasma first wall. Oxygen gettering properties and hydrogen retention properties

L163 ANSWER 13 OF 20 HCA COPYRIGHT 2002 ACS

TI Heat-treatment apparatus for **semiconductor wafer process**

L163 ANSWER 14 OF 20 HCA COPYRIGHT 2002 ACS

TI Boronization experiments and surface characterization of boron films

L163 ANSWER 15 OF 20 HCA COPYRIGHT 2002 ACS

TI Die-casting **process** and equipment suitable for aluminum-silicon alloys

L163 ANSWER 16 OF 20 HCA COPYRIGHT 2002 ACS

TI Ceramic particle-dispersed titanium alloy parts for injection in die casting

L163 ANSWER 17 OF 20 HCA COPYRIGHT 2002 ACS

TI Injection apparatus for hot **chamber**-type die-casting machines

L163 ANSWER 18 OF 20 HCA COPYRIGHT 2002 ACS

TI Process for purifying nitrogen trifluoride gas

L163 ANSWER 19 OF 20 HCA COPYRIGHT 2002 ACS

TI Cooled apparatus for vapor-phase deposition

L163 ANSWER 20 OF 20 HCA COPYRIGHT 2002 ACS

TI Heat treatment of **container liner** for metal hot extrusion die

=> d l163 1,2,3,5,13,19 cbib abs hitind

L163 ANSWER 1 OF 20 HCA COPYRIGHT 2002 ACS

137:66804 Zirconia toughened ceramic components and coatings for plasma **chambers of semiconductor processing**

equipment and method of manufacture. O'Donnell, Robert J.; Chang, Christopher C.; Daugherty, John E. (USA). U.S. Pat. Appl. Publ. US 2002086153 A1 20020704, 11 pp. (English). CODEN: USXXCO. APPLICATION: US 2000-750056 20001229.

AB A corrosion resistant component of **semiconductor processing** equipment such as a plasma **chamber**

comprises zirconia toughened ceramic material as an outermost surface of the component. The component can be made entirely of the ceramic material or the ceramic material can be provided as a coating on a substrate such as aluminum or aluminum alloy, stainless steel, or refractory metal. The zirconia toughened ceramic can be tetragonal zirconia polycryst. (TZP) material, partially-stabilized

zirconia (PSZ), or a zirconia dispersion toughened ceramic (ZTC) such as zirconia-toughened alumina (tetragonal zirconia particles dispersed in Al₂O₃). In the case of a ceramic zirconia toughened coating, one or more intermediate layers may be provided between the component and the ceramic coating. To promote adhesion of the ceramic coating, the component surface or the intermediate layer surface may be subjected to a surface roughening treatment prior to depositing the ceramic coating.

IC ICM B32B009-00
NCL 428336000
CC 57-2 (Ceramics)
Section cross-reference(s): 47
ST zirconia toughened ceramic coating **semiconductor processing** equipment; plasma **chamber** zirconia toughened ceramic coating component
IT **Vapor deposition process**
(chem.; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Molding
(cold isostatic pressing; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Molding
(compression; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Sintering
(hot isostatic pressing; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Coating process
(immersion; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Coating materials
(**linings**; zirconia toughened **ceramic** components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Vapor deposition process
(phys.; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Coating process
(plasma spraying; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
IT Etching apparatus
Vapor deposition apparatus
(plasma; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)

- IT Surface treatment
(roughening; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT Refractory metals
(substrate; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT Coating process
(thermal spraying; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT Corrosion-resistant materials
Semiconductor device fabrication
Sputtering
(zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT Ceramic coatings
Ceramics
(zirconia-toughened; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT Aluminum alloy, base
(substrate; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT 1314-23-4, Zirconia, uses
(ceramics toughened by; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT 7429-90-5, Aluminum, processes 12597-68-1, Stainless steel, processes
(substrate; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)
- IT 1344-28-1, Aluminum oxide (Al₂O₃), uses
(zirconia-toughened ceramics; zirconia toughened ceramic components and coatings for plasma **chambers** of **semiconductor processing** equipment)

L163 ANSWER 2 OF 20 HCA COPYRIGHT 2002 ACS

137:40256 **Chamber liner** for high temperature
processing chamber for **semiconductor**

device fabrication. Frankel, Jonathan; Sivaramakrishnan, Visweswaren (USA). U.S. Pat. Appl. Publ. US 20020073922 A1 20020620, 80 pp. (English). CODEN: USXXCO. APPLICATION: US 1996-746748 19961113.

AB The present invention provides systems, methods and app. for high temp. (at least .apprx.500-800.degree.) **processing** of **semiconductor wafers** to form devices with high aspect ratios and ultra-shallow doped regions. The systems, methods

and app. of the present invention allow multiple process steps to be performed in situ in the same **chamber** to reduce total processing time and to ensure high quality processing for high aspect ratio devices. Performing multiple process steps in the same **chamber** also increases the control of the process parameters and reduces device damage. In particular, the present invention can provide high temp. deposition, heating and efficient cleaning for forming dielec. films having thickness uniformity, good gap fill capability, high d., low moisture, and other desired characteristics.

IC ICM C23C016-00
NCL 118715000
CC 76-3 (Electric Phenomena)
ST **liner** semiconductor device fabrication app
IT Cleaning
 (app.; **chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT Dielectric films
Doping
Etching apparatus
Heaters
Integrated circuits
 Linings (refractory)
Semiconductor device fabrication
Vapor deposition apparatus
 (**chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT Borophosphosilicate glasses
Silicate glasses
 (**chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT Borosilicate glasses
Phosphosilicate glasses
 (**chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT Vapor deposition apparatus
 (plasma; **chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT Aluminum alloy, base
 (**chamber liner** for high temp.
 processing chamber for **semiconductor**
 device fabrication)
IT 78-10-4, TEOS 78-40-0, Triethyl phosphate 150-46-9, Triethyl
borate 7727-37-9, Nitrogen, processes 7783-54-2, Nitrogen
fluoride (NF3) 10028-15-6, Ozone, processes
 (**chamber liner** for high temp.
 processing chamber for **semiconductor**

device fabrication)
IT 1344-28-1, Alumina, uses 7429-90-5, Aluminum, uses
(chamber liner for high temp.
processing chamber for semiconductor
device fabrication)

L163 ANSWER 3 OF 20 HCA COPYRIGHT 2002 ACS

137:9472 Corrosion-resistant protective polymer **lining** for
chamber apparatus in plasma processing of substrates. Shih,
Hong; Han, Nianci; Yuan, Jie; Sommers, Joe; Ma, Diana; Vollmer,
Paul; Willson, Michael C. (USA). U.S. Pat. Appl. Publ. US
20020066532 A1 20020606, 12 pp., Cont. of U. S. Ser. No. 532,343.
(English). CODEN: USXXCO. APPLICATION: US 2001-33115 20011022.
PRIORITY: US 1999-290969 19990413; US 2000-532343 20000321.

AB The corrosion-resistant protective coating is applied in a
chamber app. used for substrate processing with corrosive
gas or plasma, optionally in the presence of **ceramic**
lining on the interior **chamber** wall made of Al.
The protective coating (or a sealant **lining**) is preferably
based on a polymer resulting from a monomeric anaerobic chem. mixt.
cured in a vacuum for the absence of O₂ atm. The polymer coating is
based on a major proportion of a methacrylate compd., and a minor
part of an activator to initiate the curing process of monomeric
anaerobic mixt. The typical anaerobic mixt. contains 30-95%
tetraethylene glycol dimethacrylate, 4-50% hydroxyethyl
methacrylate, and 1-5% of suitable activator (esp. cumene
hydroperoxide).

IC ICM C23F001-02

NCL 156345100

CC 56-6 (Nonferrous Metals and Alloys)

Section cross-reference(s): 38, 76

ST plasma **chamber** wall anticorrosion **lining**
polymer; methacrylate polymer **lining chamber** app
plasma etching

IT Polymerization
(anaerobic, coating by; corrosion-resistant polymer
lining for vacuum-**chamber** app. in plasma
processing)

IT Plasma
(**chamber** app. for, coating of; corrosion-resistant
polymer **lining** for vacuum-**chamber** app. in
plasma processing)

IT Vapor deposition process
(chem., **chamber** app. for, **lining**
in; corrosion-resistant polymer **lining** for vacuum-
chamber app. in plasma processing)

IT Etching
(corrosive gas, **chamber** app. for; corrosion-resistant
polymer **lining** for vacuum-**chamber** app. in
plasma processing)

IT 7429-90-5, Aluminum, uses
(**chamber** app, coating of; corrosion-resistant polymer

- lining for vacuum-chamber app. in plasma processing)
- IT 1344-28-1, Alumina, uses
(film, chamber wall with; corrosion-resistant polymer lining for vacuum-chamber app. in plasma processing)
- IT 80-15-9, Cumene hydroperoxide
(hardener, polymn. coating with; corrosion-resistant polymer lining for vacuum-chamber app. in plasma processing)
- IT 409-21-2, Silicon carbide (SiC), uses 1314-23-4, Zirconia, uses 10043-11-5, Boron nitride, uses 12033-89-5, Silicon nitride, uses 12069-32-8, Boron carbide (B4C) 24304-00-5, Aluminum nitride
(interlayer, plasma-chamber wall with; corrosion-resistant polymer lining for vacuum-chamber app. in plasma processing)
- IT 109-17-1, Tetraethylene glycol dimethacrylate 868-77-9
(polymn. coating from; corrosion-resistant polymer lining for vacuum-chamber app. in plasma processing)

L163 ANSWER 5 OF 20 HCA COPYRIGHT 2002 ACS

136:94543 **Semiconductor processing** equipment having

improved particle performance using ceramics. Bosch, William Frederick (Lam Research Corporation, USA). PCT Int. Appl. WO 2002003427 A2 20020110, 40 pp. DESIGNATED STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2001-US20284 20010625. PRIORITY: US 2000-607922 20000630.

- AB A ceramic part having a surface exposed to the interior space, the surface having been shaped and plasma conditioned to reduce particles thereon by contacting the shaped surface with a high intensity plasma. The ceramic part can be made by sintering or machining a chem. deposited material. During **processing** of **semiconductor** substrates, particle contamination can be minimized by the ceramic part as a result of the plasma conditioning treatment. The ceramic part can be made of various materials such as alumina, SiO₂, quartz, C, Si, Si carbide, Si nitride, B nitride, B carbide, Al nitride or Ti carbide. The ceramic part can be various parts of a vacuum processing **chamber** such as a **liner** within a sidewall of the processing **chamber**, a gas distribution plate supplying the process gas to the processing **chamber**, a baffle plate of a showerhead assembly, a wafer passage insert, a focus ring surrounding the substrate, an edge ring surrounding an electrode, a plasma screen and/or a window.

IC ICM H01L021-00

CC 76-3 (Electric Phenomena)

- Section cross-reference(s): 57
- ST **c ramic lining** semiconductor fabrication app
- IT Semiconductor device fabrication
(app.; **semiconductor processing** equipment
having improved particle performance using ceramics)
- IT Hydrocarbons, processes
(fluoro, plasma agent for ceramic; **semiconductor processing** equipment having improved particle performance
using ceramics)
- IT Halogens
(plasma agent for ceramic; **semiconductor processing** equipment having improved particle performance
using ceramics)
- IT **Etching** apparatus
Reactors
(plasma; **semiconductor processing** equipment
having improved particle performance using ceramics)
- IT Electric discharge devices
Holders
Linings (refractory)
Machining
Sintering
Vacuum chambers
Windows
(**semiconductor processing** equipment having
improved particle performance using ceramics)
- IT Plasma
(**treating** ceramic; **semiconductor processing** equipment having improved particle performance
using ceramics)
- IT 7782-41-4, Fluorine, processes 7782-44-7, Oxygen, processes
(plasma agent for ceramic; **semiconductor processing** equipment having improved particle performance
using ceramics)
- IT 409-21-2, Silicon carbide SiC, uses 1344-28-1, Alumina, uses
7440-21-3, Silicon, uses 7440-44-0, Carbon, uses 7631-86-9,
Silica, uses 7782-42-5, Graphite, uses 10043-11-5, Boron
nitride, uses 12033-89-5, Silicon nitride, uses 12069-32-8,
Boron carbide 12070-08-5, Titanium carbide 24304-00-5, Aluminum
nitride
(**semiconductor processing** equipment having
improved particle performance using ceramics)

L163 ANSWER 13 OF 20 HCA COPYRIGHT 2002 ACS

123:100047 Heat-treatment apparatus for **semiconductor**

wafer process. Kirino, Yoshio; Yoshikawa,
Atsushi; Chaki, Katsuhiro (Toshiba Ceramics Co, Japan). Jpn. Kokai
Tokkyo Koho JP 07058094 A2 19950303 Heisei, 4 pp. (Japanese).
CODEN: JKXXAF. APPLICATION: JP 1993-225090 19930818.

AB The title app. comprises a process **chamber** in which the
metal surface coming in contact with the reactive gas is coated with
a ceramic material, by CVD or ion plating.

- IC ICM H01L021-31
ICS H01L021-205; H01L021-22; H01L021-324
- CC 76-3 (Electric Phenomena)
- ST **semiconductor wafer process app**
ceramic lined
- IT **Semiconductor devices**
(heat-treatment app. for **semiconductor wafer process**)
- IT Vapor deposition processes
(liq.-phase; heat-treatment app. for **semiconductor wafer process**)
- IT Vapor deposition processes
(ion plating, liq.; heat-treatment app. for **semiconductor wafer process**)
- IT 7440-21-3, Silicon, uses 12627-33-7, Titanium carbide nitride
25583-20-4, Titanium nitride
(heat-treatment app. for **semiconductor wafer process**)
- L163 ANSWER 19 OF 20 HCA COPYRIGHT 2002 ACS
- 108:117302 Cooled apparatus for vapor-phase deposition. Oyama, Katsumi; Hikima, Hitoshi; Takami, Katsumi (Hitachi Electronics Engineering Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 62280367 A2 19871205 Showa, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1986-125006 19860530.
- AB The cooled app. suitable for **chem.-vapor deposition** of Si is designed to improve cooling efficiency for uniform temp. distribution. The app. has a conical cover laid on a wall ring on a **reactor** top. The cover and ring are externally **lined** with a mixt. of epoxy resin binder and Al or Cu powder, and cooled with circulating fluid in pipe placed in the **lining** beneath a thermally insulating cover. Reacting gas streams are fed downward through pipes passed through the tip of cone-shaped cover, and distributed peripherally toward substrates.
- IC ICM C23C016-44
ICS H01L021-31
- CC 56-6 (Nonferrous Metals and Alloys)
Section cross-reference(s): 47, 76
- ST **chem vapor deposition** silicon cooling;
aluminum powder resin lining app; copper powder
resin **lining app**; epoxy resin metal powder **lining**
- IT Epoxy resins, uses and miscellaneous
(binders, powd. metals in, for thermally conductive
linings of chem.-vapor deposition app.)
- IT **Linings**
(composite, on **chem.-vapor deposition**
app., high cooling efficiency and uniform temp. distribution by)
- IT Coating process
(chem.-vapor, app., composite **lining** on, for high
cooling efficiency and uniform temp. distribution)
- IT 7429-90-5, Aluminum, uses and miscellaneous 7440-50-8, Copper,

uses and miscellaneous
(powder, **linings** from resin-bonded, on **chem.-**
vapor deposition app.)

=> d 1177 1-14 ti

L177 ANSWER 1 OF 14 HCA COPYRIGHT 2002 ACS

TI Free floating shield for reducing film deposition on the
processing equipment and **semiconductor**
processing system including the shield

L177 ANSWER 2 OF 14 HCA COPYRIGHT 2002 ACS

TI Actively-cooled distribution plate for reducing reactive gas
temperature in a plasma processing system

L177 ANSWER 3 OF 14 HCA COPYRIGHT 2002 ACS

TI A six-wafer combustion system for a silicon micro gas turbine engine

L177 ANSWER 4 OF 14 HCA COPYRIGHT 2002 ACS

TI Free floating shield and **semiconductor** gas
processing system

L177 ANSWER 5 OF 14 HCA COPYRIGHT 2002 ACS

TI Free floating shield

L177 ANSWER 6 OF 14 HCA COPYRIGHT 2002 ACS

TI Semiconductor devices and apparatus for their manufacture

L177 ANSWER 7 OF 14 HCA COPYRIGHT 2002 ACS

TI Gas injection system for **semiconductor processing**

L177 ANSWER 8 OF 14 HCA COPYRIGHT 2002 ACS

TI Gas distribution apparatus

L177 ANSWER 9 OF 14 HCA COPYRIGHT 2002 ACS

TI Method and apparatus for **semiconductor** device
processing

L177 ANSWER 10 OF 14 HCA COPYRIGHT 2002 ACS

TI **Temperature-controlled** gas distributor for
chemical vapor deposition on glass

L177 ANSWER 11 OF 14 HCA COPYRIGHT 2002 ACS

TI Atmospheric-pressure **chemical vapor**
deposition apparatus

L177 ANSWER 12 OF 14 HCA COPYRIGHT 2002 ACS

TI Apparatus for coating the upper surface of a sheet of heated glass

L177 ANSWER 13 OF 14 HCA COPYRIGHT 2002 ACS

TI Single **wafer** plasma **etch reactor**

L177 ANSWER 14 OF 14 HCA COPYRIGHT 2002 ACS
TI Apparatus for **chemical vapor d position**

=> d l177 1,4,5,6,9,13,14 cbib abs hitind

L177 ANSWER 1 OF 14 HCA COPYRIGHT 2002 ACS
136:192853 Free floating shield for reducing film deposition on the
processing equipment and **semiconductor**
processing system including the shield. Bartholomew,
Lawrence Duane; Dedontney, Jay Brian; Peabody, Christopher A.
(Silicon Valley Group, Thermal Systems Llc, USA). U.S. US 6352592
B1 20020305, 43 pp., Cont.-in-part of U. S. 6,056,824. (English).
CODEN: USXXAM. APPLICATION: US 2000-492420 20000127. PRIORITY: US
1998-8024 19980116; US 1998-185180 19981103.

AB A protective shield and a **semiconductor processing**
system including a protective shield are provided. The shield
includes a frame assembly including a pair of spaced end walls and a
pair of side walls extending between and mounted to the end walls,
and a plurality of shield bodies carried by the frame assembly.
Each of the shield bodies includes a base having a continuous unit
frame, a perforated sheet carried by said continuous frame, a
plenum between the base and the perforated sheet, and a gas
delivery device for delivering an inert gas to the **plenum**
at a flow rate such that the gas diffuses through the perforated
sheet. The **CVD** system includes a plurality of processing
chambers, a conveyor for transporting substrates through the
processing **chambers**, buffer modules isolating the
processing **chambers** from the rest of the process path all
enclosed within a muffle, a protective shield mounted in the
processing **chambers** includes injector shield bodies
positioned adjacent the injector and shunt shield bodies spaced from
the injector shield bodies, an **inlet port**
between the injector shield bodies, and an **outlet**
port between the shunt shield bodies for the flow of
reagents through the protective shield. The shunt shield bodies
each include a **plenum** filled with an inert gas and a
bottom **outlet port** coupled to the **plenum**
for delivering a supply of inert gas below the protective shield to
form buffer barriers on opposite sides of the injection
ports. The shield body captures the perforated sheets and
shield bodies such that the sheets and shield body base can freely
expand and contract relative to each other and the end walls under
varying temp. conditions, maintaining the precise **chamber**
geometry control required for **CVD** processing. The buffer
modules are connected to a common bypass exhaust which is
independent from the system. The processing **chambers** are
connected to a common **chamber** exhaust **plenum**
which is sep. from the bypass exhaust. Such sep. exhaust paths
allow for sep. control of each and for the substantially const. flow
of gases within the system.

IC ICM C23C016-00
NCL 118719000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST free floating shield **semiconductor processing**
system
IT Shields
(**semiconductor processing** system including
free floating shield for reducing film deposition on processing
equipment)
IT Vapor deposition apparatus
(**semiconductor processing** system;
semiconductor processing system including free
floating shield for reducing film deposition on processing
equipment)

L177 ANSWER 4 OF 14 HCA COPYRIGHT 2002 ACS

132:287520 Free floating shield and **semiconductor gas**
processing system. Bartholomew, Lawrence Duane; Dedontney,
Jay Brian; Peabody, Christopher A. (Silicon Valley Group Thermal
Systems, USA). U.S. US 6056824 A 20000502, 38 pp., Cont.-in-part
of U.S. 5,849,088. (English). CODEN: USXXAM. APPLICATION: US
1998-185180 19981103. PRIORITY: US 1998-8024 19980116.

AB A protective shield and a **semiconductor processing**
system including a protective shield is provided. The shield
includes a frame assembly including a pair of spaced end walls and a
pair of side walls extending between and mounted to the end walls,
and a plurality of shield bodies carried by the frame assembly.
Each of the shield bodies includes a base having a continuous unit
frame, a perforated sheet carried by said continuous frame, a
plenum between the base and the perforated sheet, and a gas
delivery device for delivering an inert gas to the **plenum**
at a flow rate such that the gas diffuses through the perforated
sheet. The CVD system includes a plurality of processing
chambers, a conveyor for transporting substrates through the
processing **chambers**, buffer modules isolating the
processing **chambers** from the rest of the process path all
enclosed within a muffle. a protective shield mounted in the
processing **chambers** includes injector shield bodies
positioned adjacent the injector and shunt shield bodies spaced from
the injector shield bodies, an **inlet port**
between the injector shield bodies, and an **outlet**
port between the shunt shield bodies for the flow of
reagents through the protective shield. The shunt shield bodies
each include a **plenum** filled with an inert gas and a
bottom **outlet port** coupled to the **plenum**
for delivering a supply of inert gas below the protective shield to
form buffer barriers on opposite sides of the injection
ports. The shield body captures the perforated sheets and
shield bodies such that the sheets and shield body base can freely
expand and contract relative to each other and the end walls under
varying temp. conditions, maintaining the precise **chamber**

geometry control required for **CVD** processing. The buffer modules are connected to a common bypass exhaust which is independent from the system. The processing **chambers** are connected to a common **chamber** exhaust **plenum** which is sep. from the bypass exhaust. Such sep. exhaust paths allow for sep. control of each and for the substantially const. flow of gases within the system.

IC ICM C23C016-00
NCL 118719000
CC 76-3 (Electric Phenomena)
ST **CVD** app floating shield
IT Control apparatus
Semiconductor device fabrication
Shields
Vapor deposition apparatus
(free floating shield and **semiconductor** gas
processing system)

L177 ANSWER 5 OF 14 HCA COPYRIGHT 2002 ACS

130:74149 Free floating shield. Dedontney, Jay Brian; Bartholomew, Lawrence Duane (Watkins-Johnson Company, USA). U.S. US 5849088 A 19981215, 18 pp. (English). CODEN: USXXAM. APPLICATION: US 1998-8024 19980116.

AB A protective shield and an atm. pressure **CVD** system including a protective shield are given. The shield includes a frame assembly including a pair of spaced end walls and a pair of side walls extending between and mounted to the end walls, and a plurality of shield bodies carried by the frame assembly. Each of the shield bodies includes a base, a perforated sheet carried by the base, a **plenum** between the base and the perforated sheet, and a gas delivery device for delivering an inert gas to the **plenum** at a flow rate such that the gas diffuses through the perforated sheet. The **CVD** system includes a plurality of processing **chambers**, a conveyor for transporting substrates through the processing **chambers**, buffer **chambers** isolating the processing **chambers** from the rest of the process path all enclosed within a muffle. A protective shield mounted in the processing **chambers** includes injector shield bodies positioned adjacent the injector and shunt shield bodies spaced from the injector shield bodies, an **inlet port** between the injector shield bodies, and an **outlet port** between the shunt shield bodies for the flow of reagents through the protective shield. The shunt shield bodies each include a **plenum** filled with an inert gas and a bottom **outlet port** coupled to the **plenum** for delivering a supply of inert gas below the protective shield to form buffer barriers on opposite sides of the injection **ports**. The shield body captures the perforated sheets and shield bodies such that the sheets and shield body base can freely expand and contract relative to each other and the end walls under varying temp. conditions, maintaining the precise **chamb r** geometry control required for **CVD**

processing.
IC ICM C23C016-00
NCL 118719000
CC 75-1 (Crystallography and Liquid Crystals)
ST CVD system protective shield
IT Shields
(protective shield assembly for CVD systems for protecting exposed surfaces of gas injector, chamber wall or exhaust vent)
IT Vapor deposition apparatus
(shield assembly for CVD systems for protecting exposed surfaces of gas injector, chamber wall or exhaust vent)

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129:238671 Semiconductor devices and apparatus for their manufacture. Umeta, Hiroshi (Mitsubishi Electric Corp., Japan). Jpn. Kokai Tokkyo Koho JP 10229078 A2 19980825 Heisei, 9 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-33521 19970218.

AB The app. has heat treatment and reserve chambers, and the latter has a meandering path in a material between an inlet and an outlet for raising the temp. of a gas. The chambers are kept at different temps. with independent temp.-controlling means, and a thermal barrier may be placed between the chambers. The reserve chamber may have halogen lamps installed on its circumference, the material may contain SiC and/or Si, the heat treatment may include formation of a Si oxynitride on a Si substrate with supply of N2O, and the reserve chamber may have an inner vol. .gtoreq.12,600 cm3.

IC ICM H01L021-31
ICS H01L021-318; H01L021-324
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST gas preheating chamber semiconductor processing app; heat treatment semiconductor device manuf; silicon oxynitride formation semiconductor device manuf
IT Semiconductor device fabrication
(heat treatment with supply of reaction gases preheated in reserve chambers in)
IT Heat pipes
(heating pipes; for preheating of reaction gases in reserve chambers in manuf. of semiconductor devices)

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122:304520 Method and apparatus for semiconductor device processing. Moslehi, Mehrdad M. (Texas Instruments Inc., USA). Eur. Pat. Appl. EP 641017 A1 19950301, 17 pp. DESIGNATED STATES: R: DE, FR, GB, IT, NL. (English). CODEN: EPXXDW. APPLICATION: EP 1994-113310 19940825. PRIORITY: US 1993-114887 19930831.

AB A multipurpose app. has a chamber for holding a medium.

The medium is heated into the molten state by a radio-frequency induction heating coil. The medium heats a semiconductor material through a chuck member that encloses 1 end of the **chamber** and separates the medium from the semiconductor material. The heating performed by the coil generates a fluid flow within the medium, providing a uniform temp. distribution throughout the medium. A magnetic rotation device controls the movement of a rotating member having a mixing member and rotating fins to ensure complete uniform temp. distribution throughout the medium, esp. in the vicinity of the chuck member. An **inlet** cooling tube and an **outlet** cooling tube, isolated from the medium, provide cooling fluid to the chuck member for **temp. control** of the semiconductor material.

IC ICM H01L021-00
 CC 76-3 (Electric Phenomena)
 ST **semiconductor device processing** method app;
 chuck member **semiconductor device processing**
 app; induction heater **semiconductor device**
processing app
 IT Heating systems and Heaters
 (induction, **semiconductor device processing**
 app. contg.)

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 103:114637 Single **wafer** plasma **etch reactor**

. Chen, Lee; Hendricks, Charles J.; Mathad, Gangadhara S.;
 Poloncic, Stanley J. (International Business Machines Corp. , USA).
 U.S. US 4534816 A 19850813, 10 pp. (English). CODEN: USXXAM.
 APPLICATION: US 1984-623670 19840622.

AB A high-pressure, high-**etch**-rate single-**wafer**
 plasma **reactor** having a fluid cooled upper electrode
 including a plurality of small diam. holes or passages there-through
 to provide uniform reactive gas distribution over the surface of a
wafer to be **etched** is described. A fluid-cooled
 lower electrode is spaced from the upper electrode to provide an
 aspect ratio (wafer diam.: spacing) greater than .apprx.25, and
 includes an insulating ring at its upper surface. The insulating
 ring protrudes above the exposed surface of the lower electrode to
 control the electrode spacing and to provide a plasma confinement
 region whereby substantially all of the RF power is dissipated by
 the wafer. A plurality of spaced apart, radially extending passages
 through the insulating ring provide a means of uniformly exhausting
 the reactive gas from the plasma confinement region. Affixed to the
 upper electrode is a first housing which supplies reactive gas and
 cooling fluid, and a baffle affixed to the first housing
 intermediate the upper electrode and a gas **inlet** forms a
plenum above the upper electrode and ensures uniform
 reactive gas distribution thereover. The first housing and upper
 electrode are contained within a second housing with an insulating
 housing therebetween. The upper and lower electrodes are elec.
 isolated from each other and from ground, so that either or both
 electrodes may be powd. Improved etch rates and etch uniformity for

etching a variety of materials are achieved. The uniform reactive gas distribution, the extremely close spacing of the electrodes, and a high degree of plasma confinement are factors.

IC ICM H01L021-306
ICS B44C001-22; C03C015-00; C23F001-02
NCL 156345000
CC 76-11 (Electric Phenomena)
ST **semiconductor wafer** plasma **etching** app
IT Electric discharge devices
(plasma **etching**, single-wafer)
IT Sputtering
(**etching**, app., for **semiconductor** wafers
single-wafer)

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100:72709 Apparatus for **chemical vapor deposition**. (Agency of Industrial Sciences and Technology, Japan). Jpn. Kokai Tokkyo Koho JP 58167766 A2 19831004 Showa, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1982-51971 19820330.

AB The app. is composed of a **chamber** with a gas **inlet** at the bottom and a gas **outlet** at the top, a holder for base plates, and a heater attached to the holder section for **temp. control**. It is used for **chem. vapor deposition** with mixts. of carrier gases (e.g. H₂) and reaction gases or vapors (e.g. SiCl₄). A uniform coating (e.g., Si) is obtained.

IC C23C011-00
CC 56-6 (Nonferrous Metals and Alloys)
Section cross-reference(s): 47, 76
ST **vapor deposition chem** app; silicon
coating app
IT Coating process
(app., **chem. vapor deposition**, with
silicon)
IT 7440-21-3, uses and miscellaneous
(coating with, app. for **chem. vapor deposition**)